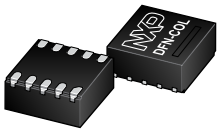


FXLS8967AF

3-Axis Low-g Accelerometer

Rev. 1.5 — 11 March 2022 Product data sheet

1 General description

FXLS8967AF is a compact 3-axis MEMS accelerometer designed for use in a wide range of automotive security and convenience applications that require ultra-low-power wake-up on motion. The part supports both high-performance and low-power operating modes, allowing maximum flexibility to meet the resolution and power needs for various unique use cases. A number of advanced, integrated digital features enable designers to reduce the overall system power consumption and simplify host data collection.

FXLS8967AF is available in a 2 mm x 2 mm x 0.95 mm 10-pin DFN package with 0.4 mm pitch and wettable flanks. The device is qualified to AEC-Q100 and operates over the extended –40 °C to +105 °C temperature range. The combination of sensor performance, system power-saving features, and extended over-temperature-range performance makes FXLS8967AF an ideal accelerometer for automotive security and convenience applications.

2 Features and benefits

- ±2/4/8/16 *g* user-selectable, full-scale measurement ranges
- 12-bit acceleration data
- 8-bit temperature sensor data
- Low noise: 230 µ*g*/√Hz in high performance mode
- Low-power capability:
  - ≤ 1 µA I_{DD} for ODRs up to 6.25 Hz
  - < 4 µA I_{DD} for ODRs up to 50 Hz
- Selectable ODRs up to 3200 Hz; Flexible Performance mode allows for custom ODRs with programmable decimation (resolution) and idle-time settings
- 144 byte output data buffer (FIFO/LIFO) capable of storing up to 32 12-bit X/Y/Z data triplets
- Flexible Sensor Data Change Detection (SDCD) function for realizing motion or no motion, high-*g*/low-*g*, freefall, and other inertial events
- Autonomous orientation detection function (Portrait/Landscape/Up/Down)
- Dedicated low-power motion-detection mode with one wire interface option
- 12-bit vector magnitude calculation
- Trigger input for synchronizing data collection with an external system
- I^2C interface frequencies up to 1 MHz; 3- and 4-wire SPI interface with clock frequencies up to 4 MHz
- Bidirectional self-test diagnostic: Device motion or orientation does not impact the result.

3 Applications

3.1 Automotive security and convenience

- Infotainment
- Telematics (T-Box)
- Car alarm
- Inclinometer
- Door checker
- SmartLock

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
FXLS8967AF	VSON10	Plastic, very thin small outline package, no leads; 10 terminals; 0.4 mm pitch; 2 mm x 2 mm x 0.95 mm body	SOT1615-3

4.1 Ordering options

Table 2. Ordering options

Part number	Temperature range	Package description	Shipping
FXLS8967AFR3	–40 °C to +105 °C	DFN-10	Tape and reel

5 Block diagram

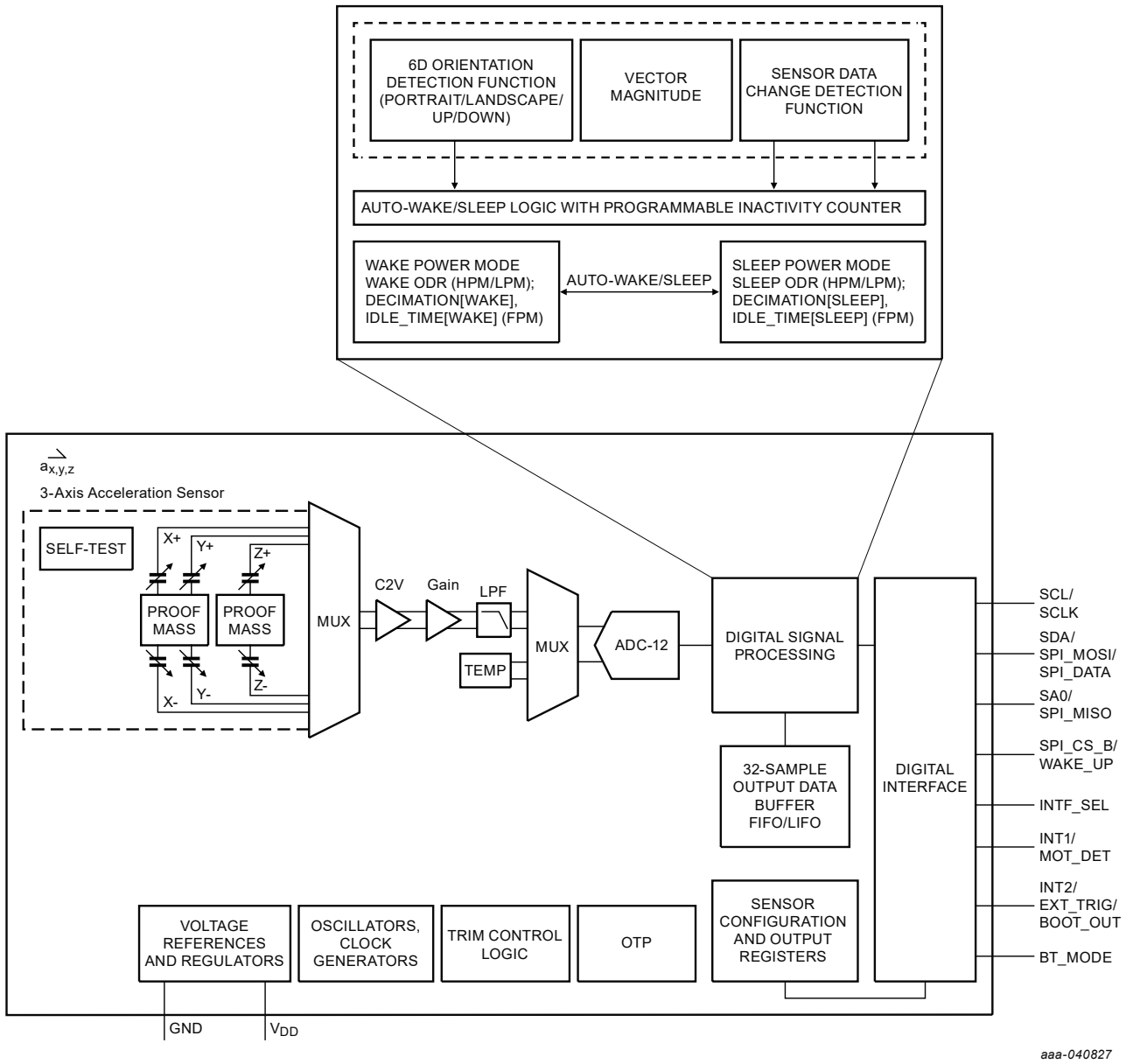


Figure 1. Block Diagram

6 Pinning information

6.1 Pinning

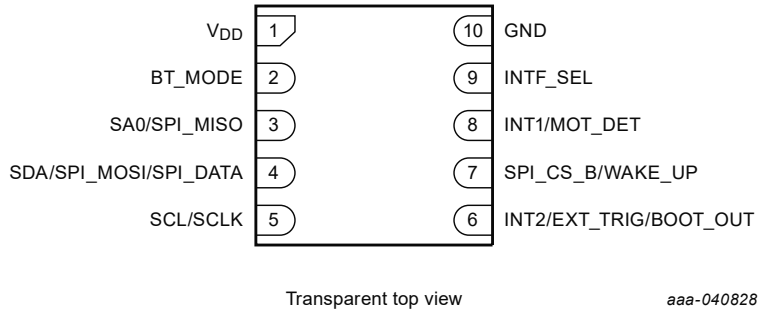


Figure 2. Pin configuration diagram

6.2 Pinning description

Table 3. Pin descriptions

Symbol	Pin	Description
V_{DD}	1	Sensor and digital interface supply voltage: 1.71 VDC to 3.6 VDC.
BT_MODE	2	Device boot mode selection.[1] GND: Default operating mode enabled V_{DD}: Motion Detection mode enabled
SA0 / SPI_MISO	3	Mode-dependent Multifunction serial interface pin.[2] INTF_SEL = V_{DD}: • SPI_MISO: In 4-wire SPI mode this pin functions as the serial data output. INTF_SEL = GND: • SA0: This pin selects the least significant bit of the device I^2C secondary address.
SDA / SPI_MOSI / SPI_DATA	4	Mode-dependent Multifunction serial interface pin.[2] INTF_SEL = V_{DD}: • SPI_MOSI: In 4-wire SPI mode this pin functions as the serial data input. • SPI_DATA[3]: In 3-wire SPI mode, this pin functions as the bidirectional serial data input/output. INTF_SEL = GND: • SDA: This pin functions as the I^2C Serial Data input/output.
SCL / SCLK	5	Mode-dependent Multifunction serial interface pin.[2] INTF_SEL = V_{DD}: • SPI serial clock input (3- and 4-wire modes) INTF_SEL = GND: • I^2C serial clock input

Table 3. Pin descriptions...*continued*

Symbol	Pin	Description
INT2 / EXT_TRIG / BOOT_OUT	6	Mode-dependent multifunction I/O pin 2.[2] BT_MODE = V_{DD}: Open-drain[4] output signaling the device boot process has completed. This pin is typically connected to MOT_DET in a wired-AND configuration; a pull-up resistor is required. BT_MODE = GND: Programmable interrupt output pin 2[5] / External measurement trigger input. This pin should be left unconnected if unused in the application circuit.
SPI_CS_B / WAKE_UP	7	SPI chip select input, active low / Hibernate mode wake-up pin.[6] The WAKE_UP function is only available when BT_MODE = GND.
INT1 / MOT_DET	8	Mode-dependent multifunction I/O pin 1.[7] BT_MODE = GND: Programmable interrupt output pin 1.[5] This pin should be left unconnected if unused in the application circuit. BT_MODE = V_{DD}: MOT_DET multifunction I/O.[4] The host MCU sets this pin high through a pull-up resistor to enable motion detection, and drives it low for greater than $T_{MOT-HIB}$ ms to disable motion detection and enter Hibernate mode. FXLS8967AF will pulse the line low for $T_{PULSE-MOT}$ ms after motion is detected. This line may also be used to select the motion detection threshold. See Section 14 for more information.
INTF_SEL	9	Device interface mode selection pin. V_{DD}: SPI interface mode [3] GND: I^2C interface mode
GND	10	Supply return connection.

[1] BT_MODE state is latched after POR.
[2] Under Hibernate mode, pin configuration is High Impedance.
[3] 3-wire SPI mode may be selected in **SENS_CONFIG1[**SPI_M**]**; 3-wire operation is also possible by directly connecting the SPI_MISO and SPI_MOSI pins together on the PCB.
[4] An external pull-up resistor is required on this pin when BT_MODE = V_{DD}.
[5] This pin is configurable as either an input or output (push-pull or open-drain/open-source output type), but defaults to a push-pull output after POR, or after exiting Hibernate mode.
[6] Under Hibernate mode, pin configuration is High Impedance (when BT_MODE = V_{DD}) and CMOS Input (when BT_MODE = GND).
[7] Under Hibernate mode, pin configuration is High Impedance (when BT_MODE = GND) and CMOS Input (when BT_MODE = V_{DD}).

6.3 Orientation

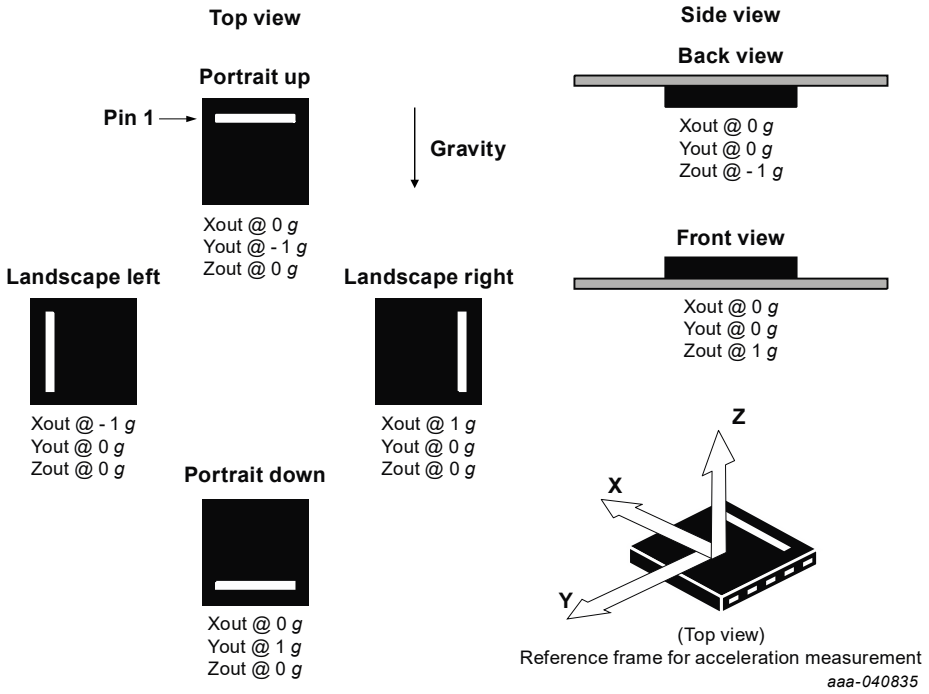


Figure 3. Sensitive axes orientation and output response to ±1 *g* (gravity) stimulus

7 Limiting values

The limiting values are the absolute maximum ratings the device can be exposed to without damage. Functional operation at absolute maximum rating is not guaranteed.

Although this device contains circuitry to protect against damage due to high static voltage or electrostatic fields, it is advised that normal precautions be taken to avoid application of any voltage higher than the maximum-rated voltage.

Table 4. Device absolute maximum ratings

Symbol	Rating	Min	Max	Unit
$ACC_{max\text{-}2k}$	Maximum applied acceleration, 0.5 ms duration	—	2,000	*g*
$ACC_{max\text{-}10k}$	Maximum applied acceleration, 0.1 ms duration	—	10,000	*g*
VDD_{MAX}	Maximum sensor supply voltage	0	+3.6	V
VIN_{MAX}	Maximum voltage level applied to any input pin	–0.3	VDD+0.3	V
T_{OP}	Operating temperature range	–40	+105	°C
T_{STG}	Storage temperature range	–40	+125	°C

Table 5. ESD and latch-up-protection characteristics

Symbol	Rating	Min	Unit
V_{HBM}	Human Body Model	±2000	V
V_{CDM}	Charged Device Model	±500	V
I_{LU}	Latch-up current at T = +105 °C (per AEC-Q100-004)	±100	mA

CAUTION

This device is sensitive to mechanical shock. Improper handling can cause permanent damage to the part or cause the part to otherwise fail.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

8 Recommended operating conditions

Table 6. Nominal operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.71	3.0	3.6	V
Top	Operating temperature range	–40	+25	+105	°C

9 Mechanical characteristics

Table 7. Accelerometer sensor performance parameters

V_{DD} = 1.8 V to 3.0 V, T = –40 °C to 105 °C, unless otherwise noted.

Typical values represent mean or mean ±1 σ values, depending on the specific parameter.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
n_{ACC}	Output data width	—	—	12	—	bits
FSR	Full-scale measurement range	±2 *g* mode	—	±2	—	*g*
		±4 *g* mode	—	±4	—	
		±8 *g* mode	—	±8	—	
		±16 *g* mode	—	±16	—	

Table 7. Accelerometer sensor performance parameters*...continued*

V_{DD} = 1.8 V to 3.0 V, T = –40 °C to 105 °C, unless otherwise noted.

Typical values represent mean or mean ±1 σ values, depending on the specific parameter.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SEN	Nominal sensitivity	±2 *g* mode	0.87	0.98	1.12	mg/LSB
		±4 *g* mode	1.74	1.95	2.23	
		±8 *g* mode	3.47	3.91	4.46	
		±16 *g* mode	6.94	7.81	8.93	
		±2 *g* mode	896	1024	1152	LSB/*g*
		±4 *g* mode	448	512	576	
		±8 *g* mode	224	256	288	
		±16 *g* mode	112	128	144	
SEN_{TOL}	Sensitivity tolerance[1]	—	—	±2.5	—	%SEN
TCS	Temperature coefficient of sensitivity[1]	–40 °C to +105 °C	—	±0.01	—	%/°C
OFF_{PBM}	Zero-*g* offset, post-board mount, FSR ≤ ±8*g*[1][2]	XY axes	–200	±50	200	m*g*
		Z axis	–550	±150	550	
TCO_{PBM}	Zero-*g* offset temperature coefficient, post-board mount[1]	XY axes	—	0.55	—	mg/°C
		Z axis	—	0.8	—	
CAS	Cross-axis sensitivity[3]	±2/4 *g* mode	—	±0.5	—	%
STOC	Self-test output change[4]	±4 *g* mode, X axis	–206	–139	–81	LSB
		±4 *g* mode, Y axis	78	137	207	
		±4 *g* mode, Z axis	–727	–448	–120	
		±8 *g* mode, X axis	–103	–69	–40	
		±8 *g* mode, Y axis	38	68	103	
		±8 *g* mode, Z axis	–355	–223	–71	
		±16 *g* mode, X axis	–52	–35	–19	
		±16 *g* mode, Y axis	19	34	52	
		±16 *g* mode, Z axis	–178	-112	–35	
STOF	Self-test offset[4]	±4 *g* mode	–1600	—	+1600	LSB
		±8 *g* mode	–800	—	+800	
		±16 *g* mode	–400	—	+400	
BW_{MAX}	Maximum signal bandwidth	ODR = 3200 Hz	—	1600	—	Hz
ODR_{MAX}	Maximum ODR	—	—	3200	—	Hz
NSD_{HPM}	Noise Spectral Density, High Performance Mode, FSR ≤ ±4 g, 25 Hz ≤ ODR ≤ 3200 Hz	XY axes	—	217	—	µg/√Hz
		Z axis	—	257	—	
$NRMS_{LPM}$	Noise RMS, Low-Power Mode, FSR ≤ ±4 g, all ODR ranges[5]	XY axes	—	7.8	—	mg
		Z axis	—	9.4	—	

[1] Determined with post board mount data using a standard lead-free reflow profile and NXP recommended landing pattern on a 2-layer FR4 PCB with 1.2 mm (47 mil) overall thickness.
[2] Based on characterization data on limited number of parts from 3 lots
[3] See Cross-axis sensitivity in Section 20 "Glossary".
[4] See Self-Test in Section 20 "Glossary"
[5] In low-power mode, higher ODR settings result in a lower noise density figure.

10 Electrical characteristics

Table 8. Electrical characteristics

V_{DD} = 1.8 V to 3.0 V, T = –40 °C to 105 °C, unless otherwise noted.
Typical values represent mean or mean ±1 σ values, depending on the specific parameter.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	—	1.71	3.0	3.6	V
IDD_{HPM}	Average current draw in High Performance mode	ODR independent, T = 25 °C	—	150	200	µA
IDD_{LPM}	Average current draw in low-power mode	ODR = 3200 Hz, T = 25 °C	—	150	200	µA
		ODR = 1600 Hz, T = 25 °C	—	75	100	
		ODR = 800 Hz, T = 25 °C	—	38	53	
		ODR = 400 Hz, T = 25 °C	—	20	30	
		ODR = 200 Hz, T = 25 °C	—	11	20	
		ODR = 100 Hz, T = 25 °C	—	5.3	10	
		ODR = 50 Hz, T = 25 °C	—	3.1	7	
		ODR = 25 Hz, T = 25 °C	—	1.8	4	
		ODR = 12.5 Hz, T = 25 °C	—	1.4	2.5	
		ODR = 6.25 Hz, T = 25 °C	—	1.0	2.0	
		ODR = 3.125 Hz, T = 25 °C	—	0.80	1.5	
		ODR = 1.563 Hz, T = 25 °C	—	0.70	1.5	
		ODR = 0.781 Hz, T = 25 °C	—	0.65	1.5	
IDD_{STBY}	Supply current draw in Standby mode	T = 25 °C	—	0.60	1.5	µA
IDD_{HIB}	Supply current draw in Hibernate mode	T = 25 °C	—	15	100	nA

Table 8. Electrical characteristics...*continued*

V_{DD} = 1.8 V to 3.0 V, T = –40 °C to 105 °C, unless otherwise noted.

Typical values represent mean or mean ±1 σ values, depending on the specific parameter.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IDD_{HPM}	Average current draw in High Performance mode	ODR independent	—	—	200	µA
IDD_{LPM}	Average current draw in low-power mode	ODR = 3200 Hz	—	—	200	µA
		ODR = 1600 Hz	—	—	100	
		ODR = 800 Hz	—	—	53	
		ODR = 400 Hz	—	—	30	
		ODR = 200 Hz	—	—	25	
		ODR = 100 Hz	—	—	13	
		ODR = 50 Hz	—	—	10	
		ODR = 25 Hz	—	—	8	
		ODR = 12.5 Hz	—	—	4	
		ODR = 6.25 Hz	—	—	4	
		ODR = 3.125 Hz	—	—	4	
		ODR = 1.563 Hz	—	—	4	
		ODR = 0.781 Hz	—	—	4	
IDD_{STBY}	Supply current draw in Standby mode	—	—	—	4	µA
IDD_{HIB}	Supply current draw in Hibernate mode	T = –40 °C to +85 °C	—	—	300	nA
		T = 105 °C	—	—	2	µA
VIH	High-level input voltage: SCL/SCLK, SDA/SPI_MOSI/SPI_DATA, SA0, INTF_SEL, BT_MODE, SPI_CS_B/WAKE_UP, MOT_DET, EXT_TRIG pins	—	0.7 * V_{DD}	—	—	V
VIL	Low-level input voltage: SCL/SCLK, SDA/SPI_MOSI/SPI_DATA, SA0, INTF_SEL, BT_MODE, SPI_CS_B/WAKE_UP, MOT_DET, EXT_TRIG pins	—	—	—	0.3 * V_{DD}	V
VOH	High-level output voltage: INT1/MOT_DET, INT2/BOOT_OUT, SPI_MISO, SPI_DATA pins	Io = 500 µA	0.9 * V_{DD}	—	—	V
VOL	Low-level output voltage: INT1/MOT_DET, INT2/BOOT_OUT, SPI_MISO, SPI_DATA pins	Io = 500 µA	—	—	0.1 * V_{DD}	V
$VOL_{SDA, SCL}$	Low-level output voltage on SDA and SCL pins	Io = 5 mA	—	—	0.4	V
$T_{PULSE-MOT}$	Motion detected interrupt pulse width	BT_MODE = V_{DD}	4.55	5	5.56	ms
$T_{MOT-HIB}$	MOT_DET pin low time before entering Hibernate mode[1]	BT_MODE = V_{DD}	0.91	1	6.8	ms

Table 8. Electrical characteristics...*continued*

V_{DD} = 1.8 V to 3.0 V, T = –40 °C to 105 °C, unless otherwise noted.

Typical values represent mean or mean ±1 σ values, depending on the specific parameter.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{PULSE-WIN}$	Motion detection threshold setting pulse window	BT_MODE = V_{DD}, MOT_DET = HIGH	4.55	5	5.56	ms
$T_{PULSE-THRES1}$	Motion detection threshold selection 1 – Pulse width range	BT_MODE = V_{DD}	562.5	625	883	µs
$T_{PULSE-THRES2}$	Motion detection threshold selection 2 – Pulse width range	BT_MODE = V_{DD}	1125	1250	1570	µs
$T_{PULSE-THRES3}$	Motion detection threshold selection 3 – Pulse width range	BT_MODE = V_{DD}	2250	2500	2950	µs
$T_{PULSE-DRDY}$	DRDY interrupt output pulse width	BT_MODE = GND	29	32	35.6	µs
$T_{PULSE-BOOT1}$	BOOT interrupt output pulse width	BT_MODE = GND	58	64	71.2	µs
$T_{PULSE-BOOT2}$		BT_MODE = V_{DD}	9	10	11.2	ms
ODR_{TOL}	Output Data Rate frequency tolerance	—	–10	±2.5	10	%ODR
$T_{FLT-MOT\_DET}$	MOT_DET pin deglitch filter time	BT_MODE = V_{DD}	—	10	—	µs
$T_{FLT-WAKE\_UP}$	MOT_DET, WAKE_UP pin deglitch filter time (transition out of Hibernate mode)	BT_MODE = GND, SPI_CS_B / WAKE_UP pin	—	400	—	ns
		BT_MODE = V_{DD}, MOT_DET pin	—	850	—	
T_{BOOT1}	Time needed to enter Standby mode after POR or soft reset	BT_MODE = GND	—	—	1	ms
T_{BOOT2}	Time needed to enter Motion Detection mode after POR or soft reset	BT_MODE = V_{DD}, MOT_DET = 1	—	—	17.7	ms
IDD_{BOOT}	Boot sequence peak current draw	T = –40 °C to +105 °C; with no decoupling capacitors on V_{DD} pin	—	—	5	mA
T_{ON}	Transition time (Standby mode to Active mode with valid data output)	—	—	528.5 µs + 0.9984 * (DEC – 1) * (1/(ODR * DEC))[2]	—	s
T_{OP}	Operating temperature range	—	–40	—	+105	°C

[1] Max spec covers the situation where an interrupt pulse is issued by the sensor at the same time the host MCU drives MOT_DET low to signal a hibernate command. In that case, their durations add up.

[2] DEC = decimation factor. The selected ODR and operating mode determines the decimation factor. See Section 15.13 for more information on setting or determining the measurement decimation factor. In LPM, the DEC factor is fixed at 1, making the time to first sample output fixed at 528.5 µs (typ), independent of the selected ODR.

11 Temperature sensor characteristics

Table 9. Temperature sensor performance parameters

V_{DD} = 1.8 V to 3.0 V, T = –40 °C to 105 °C, unless otherwise noted.

Typical values represent mean or mean ±1 σ values, depending on the specific parameter.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
n_{TEMP}	Output data width	—	—	8	—	bits
FSR_{TEMP}	Measurement range	—	—	–40 to +105	—	°C
SEN_{TEMP}	Sensitivity	—	—	1	—	°C/LSB
$SEN_{TOL-TEMP}$	Sensitivity tolerance	—	—	±2.5	—	%
OFF_{TEMP}	Nominal zero-output offset	Output Code = 00h	—	25	—	°C

12 I²C digital interface

The registers embedded within FXLS8967AF may be accessed using an I²C interface when the INTF_SEL pin is tied to GND. If the V_{DD} supply is not present, the device is in shutdown mode and any communications on the interface are ignored. When the device is on a common I²C-bus with other secondary devices, the V_{DD} supply pin must be left unconnected (high-impedance) when the device supply is turned off to ensure that the internal ESD protection diodes do not become forward biased and prevent the bus from functioning normally (clamping).

The I²C secondary interface port of FXLS8967AF is compliant with the following three operating modes as defined in UM10204[3]:

- Fast-mode Plus (Fm+) at 1000 kHz
- Fast-mode (Fm) at 400 kHz
- Standard-mode (Sm) at 100 kHz

Table 10. I²C serial interface pin description

Pin Name	Pin Description
SCL	I²C serial clock (pull-up resistor is required)
SDA	I²C serial data (pull-up resistor is required)

12.1 I²C interface characteristics

The I²C secondary address (7-bit format) is set to 18h when SA0 = 0, and 19h when SA0 = 1.

Table 11. FXLS8967AF I²C read and write addresses

SA0	I²C write address	I²C read address
0	30h (0011 0000b)	31h (0011 0001b)
1	32h (0011 0010b)	33h (0011 0011b)

Table 12. I^2C secondary timing values for Standard-mode (Sm), Fast-mode (Fm), and Fast-mode Plus (Fm+)

Parameter	Symbol	I^2C Standard-mode[1]		I^2C Fast-mode[1]		I^2C Fast-mode Plus[2]		Unit
		Min	Max	Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	0	1000	kHz
Bus free time between STOP and START conditions	t_{BUF}	4.7	—	1.3	—	0.5	—	µs
Repeated START hold time	$t_{HD;STA}$	4	—	0.6	—	0.26	—	µs
Repeated START setup time	$t_{SU;STA}$	4.7	—	0.6	—	0.26	—	µs
STOP condition setup time	$t_{SU;STO}$	4	—	0.6	—	0.26	—	µs
SDA valid time[3]	$t_{VD;DAT}$	—	3.45[4]	—	0.9[4]	—	0.45[4]	µs
SDA valid acknowledge time[5]	$t_{VD;ACK}$	—	3.45[4]	—	0.9[4]	—	0.45[4]	µs
SDA setup time	$t_{SU;DAT}$	250	—	100[6]	—	50	—	ns
SCL clock low time	t_{LOW}	4.7	—	1.3	—	0.50	—	µs
SCL clock high time	t_{HIGH}	4.0	—	0.6	—	0.26	—	µs
SDA and SCL risetime	t_r	—	1000	20	300	—	120	ns
SDA and SCL fall time[7][8]	t_f	—	300	—	300	—	120	ns
Pulse width of spikes on SDA and SCL (suppressed by the input filter)	t_{SP}	0	50	0	50	0	50	ns

[1] All values referred to VIH(min) and VIL(max) levels.
[2] Should be backward compatible with Fast mode.
[3] $t_{VD;DAT}$ referred to the time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
[4] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode respectively, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time.
[5] $t_{VD;ACK}$ = time for ACK signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
[6] A Fast-mode I^2C device can be used in a Standard mode I^2C system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. Also the acknowledge timing must meet this set-up time.
[7] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. The maximum fall time allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
[8] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this specified fall time when considering bus timing.

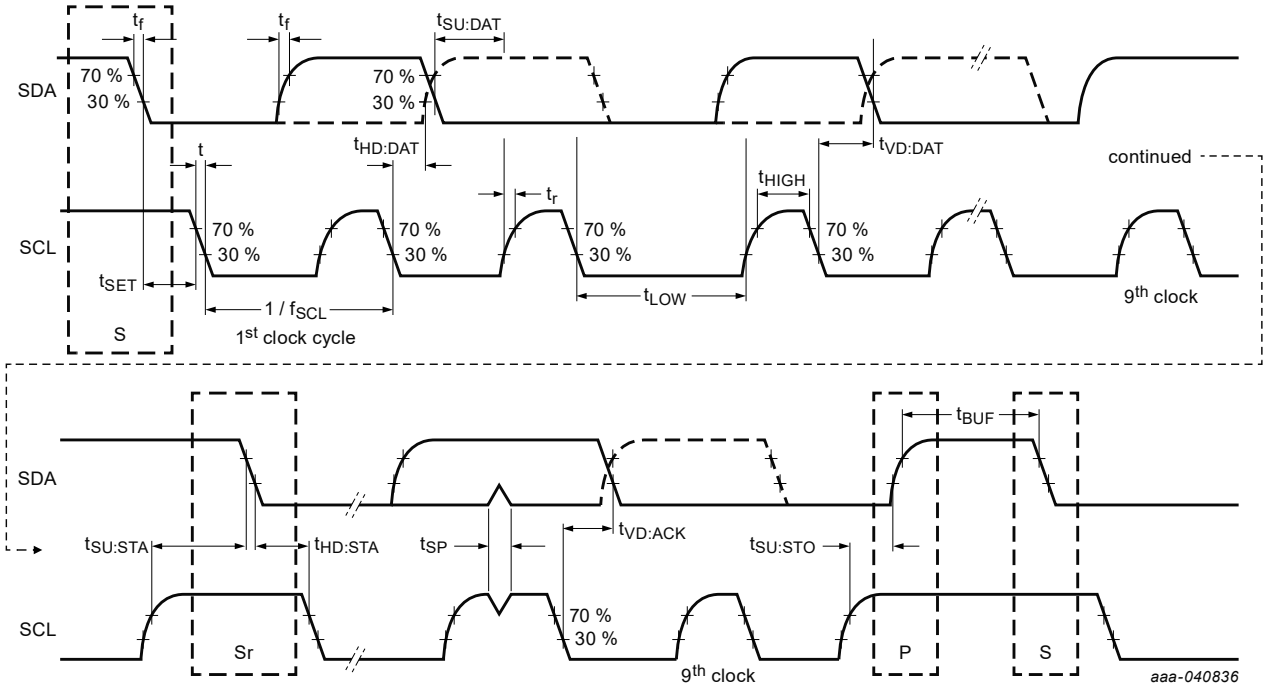


Figure 4. I^2C secondary timing diagram for Standard-mode, Fast-mode and Fast-mode Plus

12.1.1 General I^2C operation

There are two signals associated with the I^2C-bus: the Serial Clock Line (SCL) and the Serial Data line (SDA). SDA is a bidirectional signal used for sending and receiving the data to/from the interface. External pull-up resistors connected to V_{DD} are required for SDA and SCL. When the I^2C-bus is free, SCL and SDA are high.

The maximum practical operating frequency for I^2C in a given system implementation depends on several factors including the pull-up resistor and voltage values and total bus capacitance (PCB trace + parasitic device capacitances).

The primary starts a transaction on the bus through a start condition (ST) signal, which is defined as a HIGH-to-LOW transition on SDA line while the SCL line is held HIGH. After the primary transmits the ST signal, the bus is considered busy. The next byte of data transmitted contains the secondary address in the first seven bits, and the eighth bit, the read/write bit, indicates whether the primary is receiving data from the secondary or transmitting data to the secondary. When an address is sent, each device in the system compares the first seven bits after the ST condition with its own address. If they match, the device considers itself addressed by the primary. The ninth clock pulse, following the secondary address byte (and each subsequent byte) is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock period.

The number of bytes per transfer is unlimited. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the SCL line low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the clock line. This delay action is called clock stretching. Not all primary devices support clock stretching. This device implements clock stretching—the SCL line may be stretched (pulled low) for up to 1 µs when needed

during a read operation. When applied, clock stretching occurs after the ACK issued by the I^2C bus primary.

A LOW-to-HIGH transition on the SDA line while the SCL line is high is defined as a stop condition (SP) signal. The primary issuing the SP signal always terminates a write or burst write. A primary should properly terminate a read by not acknowledging a byte at the appropriate time in the protocol, followed by the SP signal. A primary may also issue a repeated start signal (SR) during a transfer.

12.1.2 I^2C read/write operations

12.1.2.1 Single-byte read

The primary transmits a start condition (ST) to FXLS8967AF, followed by the secondary address, with the R/W bit set to '0' for a write, and the FXLS8967AF sends an acknowledgment. Then the primary transmits the address of the register to read and the FXLS8967AF sends an acknowledgment. The primary transmits a repeated start condition (SR), followed by the secondary address with the R/W bit set to '1' for a read from the previously selected register. The FXLS8967AF then acknowledges and transmits the data from the requested register. The primary does not acknowledge (NAK) the transmitted data and then transmits a stop condition to end the data transfer.

12.1.2.2 Multiple-byte read

When performing a multi-byte or *burst* read, FXLS8967AF automatically increments the register read address pointer after a read command is received. Therefore, after following the steps of a single-byte read, multiple bytes of data can be read from sequential register addresses after each FXLS8967AF acknowledgment (ACK) is received. Data can be read until the primary issues a no acknowledge (NAK), followed by a stop condition (SP) signaling the end of the transfer.

12.1.2.3 Single-byte write

To start a write command, the primary transmits a start condition (ST) to the FXLS8967AF, followed by the secondary address with the R/W bit set to '0' for a write, and the FXLS8967AF sends an acknowledgment. Then the primary transmits the address of the register to write to, and the FXLS8967AF sends an acknowledgment. Then the primary transmits the 8-bit data to write to the designated register and the FXLS8967AF sends an acknowledgment signaling it has received the data. Since this transmission is complete, the primary transmits a stop condition (SP) to end the data transfer. The data sent to the FXLS8967AF is now stored in the appropriate register.

12.1.2.4 Multiple-byte write

FXLS8967AF automatically increments the register address write pointer after a write command is received. Therefore, after following the steps of a single-byte write, multiple bytes of data can be written to sequential registers after each acknowledgment (ACK) is received.

12.1.2.5 I²C data sequence diagrams

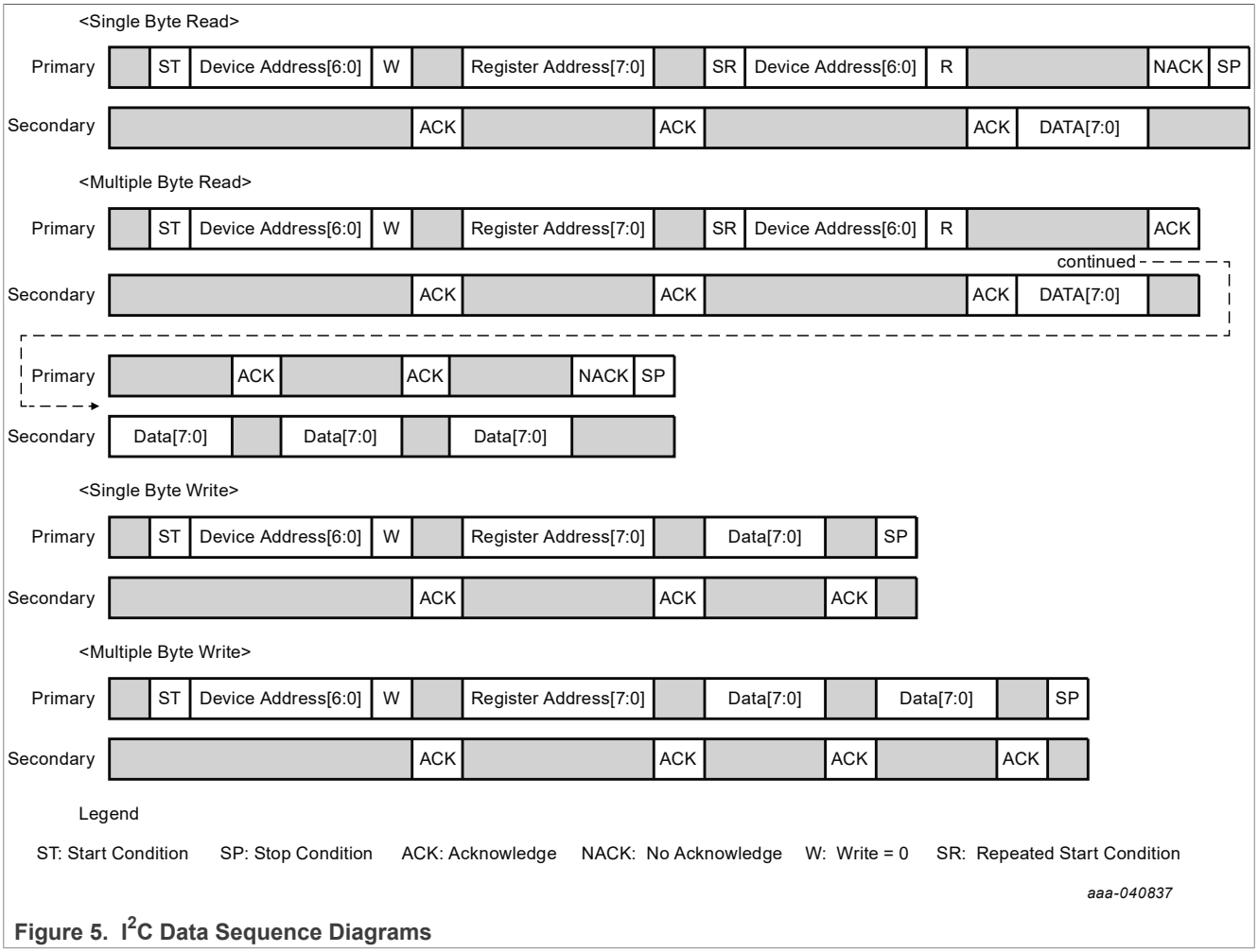


Figure 5. I²C Data Sequence Diagrams

13 SPI interface

The SPI interface is a classic primary/secondary serial port. FXLS8967AF is always considered to be the secondary device and therefore never initiates communication with the host processor.

The SPI interface of FXLS8967AF is compatible with interface mode 00, corresponding to CPOL = 0 and CPHA = 0.

For CPOL = 0, the idle value of the clock is zero, and the active value of the clock is 1. For CPHA = 0, data is captured on the rising edge (low to high transition) of the clock, and data is propagated on the falling edge (high to low transition) of the clock.

13.1 General SPI operation

The SPI_CS_B pin is driven low at the start of a transaction, held low during the transfer, and then driven high again after the transaction is completed. During a transaction, the primary toggles the clock (SCLK). The SCLK polarity is defined as having an idle value that is low, and an active phase that is high (CPOL = 0). Serial input and output data is captured on the rising edge of the clock and propagated on the falling edge (CPHA =

0). Single-byte read and single-byte write operations are completed in 24 SCLK cycles; multiple-byte reads and writes are completed in additional multiples of 8 SCLK cycles per read or written byte. The first SCLK cycle latches the R/W (Read/Write) bit to select whether the desired operation is a read (R/W = 1) or a write (R/W = 0). The following seven SCLK cycles are used to latch the register read or write address.

Note: *4-wire SPI interface mode is the default out of POR or after a soft reset. In order to select 3-wire SPI interface mode, set the* ***SENS_CONFIG1[****SPI_M****]*** *= 1.*

13.2 SPI write operations with 3- or 4-wire mode

A write operation is initiated by transmitting a 0 for the R/W bit. Then, the 7-bit register write address, A[6:0], is transmitted in MSB first order. Following this first byte, a second byte of 0s or 1s (don't care condition) transfers, followed by the actual data to write in the third group of 8 SCLK cycles (clock pulses 17 through 24) in MSB first order. Figure 6 shows the bus protocol for a single-byte register write operation in either 3- or 4-wire SPI mode.

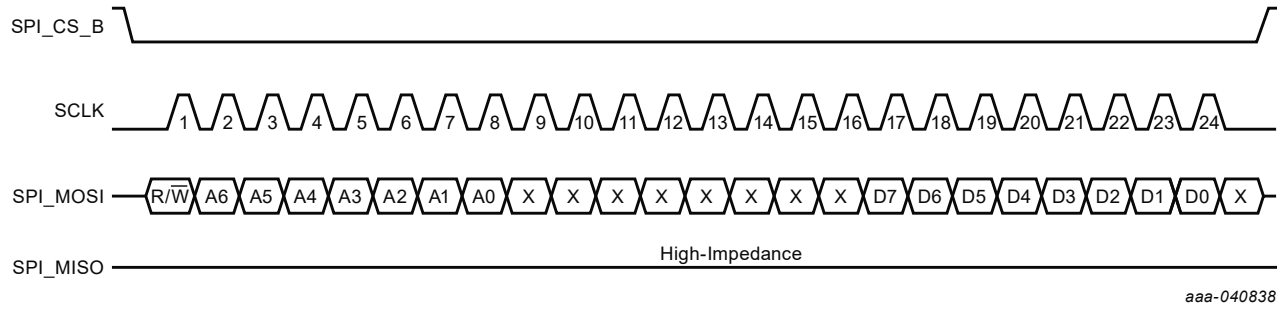


Figure 6. SPI single-byte write protocol diagram (3- or 4-wire mode), R/W = 0

Multiple-byte write operations are performed similarly to the single-byte write sequence, but with additional data bytes transferred over additional 8 SCLK cycle periods. FXLS8967AF auto-increments the register write address so that every eighth clock edge latches the address for the next register write address. When the desired number of bytes has been written, a rising edge on the SPI_CS_B pin terminates the transaction. Figure 7 shows the bus protocol for multiple-byte register write operations in either 3- or 4-wire SPI mode.

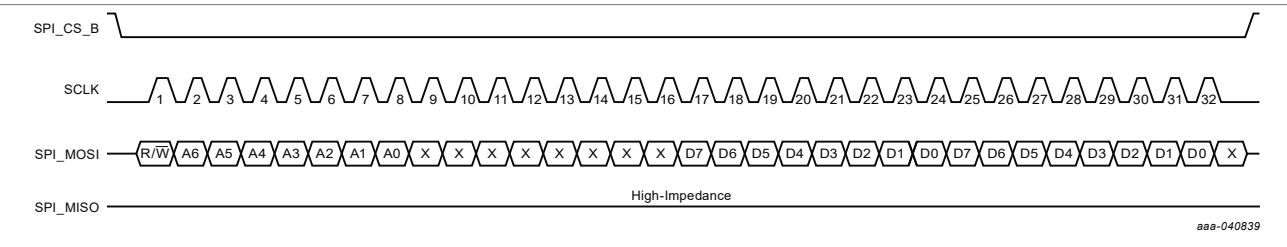


Figure 7. SPI multiple-byte write protocol diagram (3- or 4-wire mode), R/W = 0

13.3 SPI read operations with 4-wire mode

A register read operation is initiated by transmitting a 1 for the R/W bit. Then, the 7-bit register read address, A[6:0] is encoded in the first byte. Following this first byte, a second byte of 0s or 1s (don't care condition) transfers. After this transfer completes, the next 8 SCLK cycles (pulses 17 through 24) output the selected register content on the

SPI_MISO line in MSB first order. Figure 8 shows the bus protocol for a single-byte read operation.

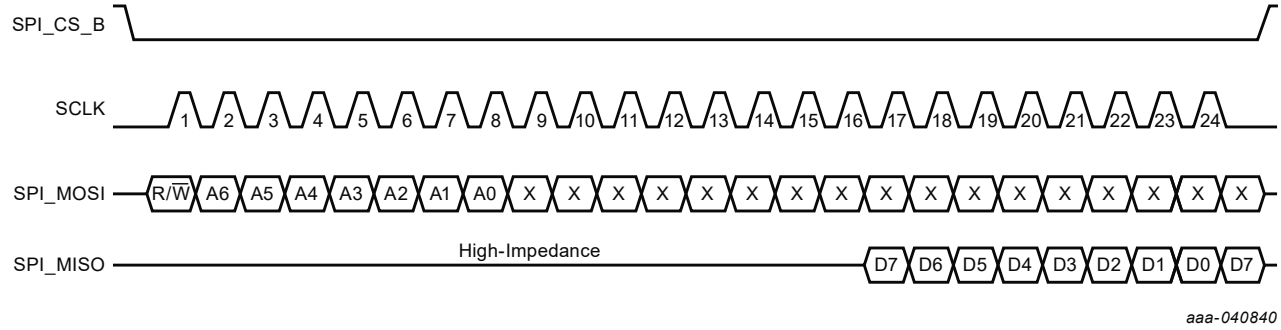


Figure 8. SPI single-byte read protocol diagram (4-wire mode), R/W = 1

Multiple-byte read operations are performed similarly to single-byte reads with additional bytes read out in multiples of eight SCLK cycles. FXLS8967AF auto-increments the register read address so that every eighth clock edge latches the address of the next sequential register read address. When the desired number of bytes has been read, a rising edge on SPI_CS_B terminates the transaction.

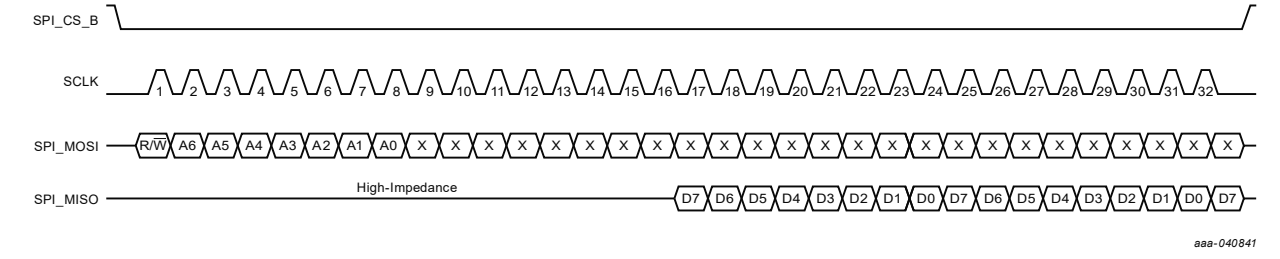


Figure 9. SPI multiple-byte read protocol diagram (4-wire mode), R/W = 1

13.4 SPI read operations with 3-wire mode

FXLS8967AF can be configured to operate in 3-wire software enabled SPI mode. In this mode, the SPI_MISO pin is left unconnected and the SPI_MOSI pin becomes a bidirectional input/output pin (SPI_DATA). Read operations in 3-wire mode are the same as write operations in 3- and 4-wire modes, except that at the end of the address cycle (falling edge of clock pulse 16), the SPI_DATA pin automatically switches from an input to an output and with bit D7 as the current output state.

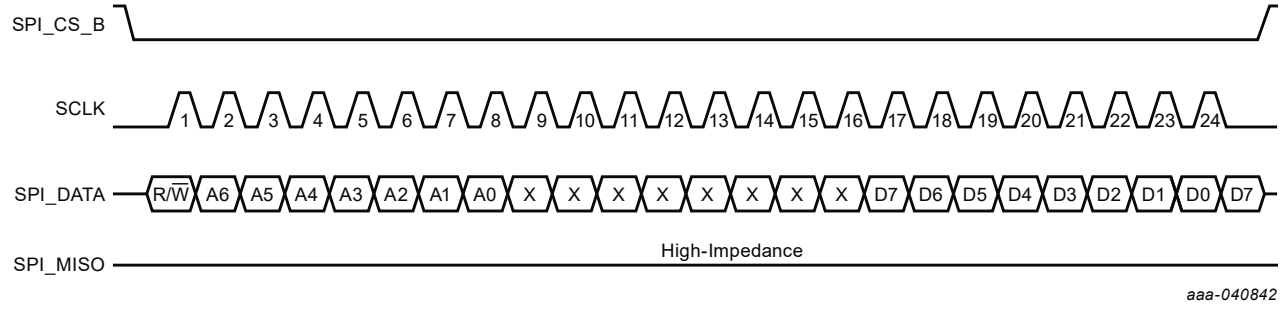


Figure 10. SPI single-byte read protocol diagram (3-wire mode)

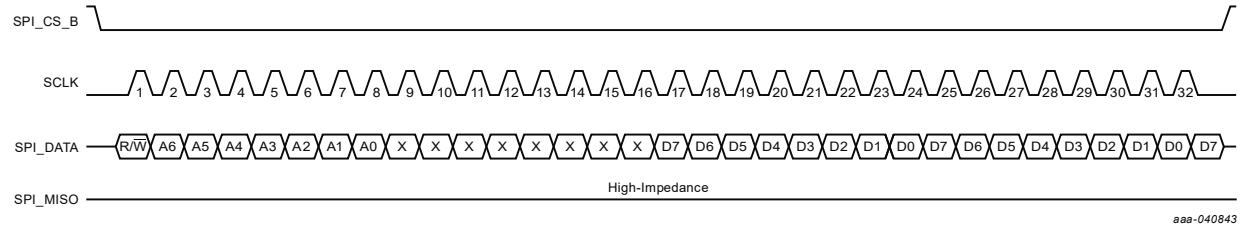


Figure 11. SPI multiple-byte read protocol diagram (3-wire mode)

13.5 SPI timing specifications (4-wire mode and 3-wire hardwired modes)

Table 13 and Figure 12 specify and illustrate the minimum and maximum timing parameter values for correct SPI interface functionality when FXLS8967AF is operated in 4-wire and 3-wire hardwired SPI modes. FXLS8967AF only supports SPI mode 00, corresponding to CPOL = 0, and CPHA = 0. In this mode, the active state of the clock is high and the idle state is low. Data is latched on the rising edge of the clock and propagated on the falling edge. All timing specifications shown in Table 13 were determined under the following conditions: 10 pF capacitor and 1 kΩ pull-up resistor present on all SPI signals, 105 °C, 1.8 V.

Table 13. Secondary timing values

Label	Description	Specifications		Unit
		Min.	Max.	
fSCLK	SCLK frequency	0	4	MHz
tSCLK	SCLK Period	250	—	ns
tSCLKH	SCLK high time	100	—	ns
tSCLKL	SCLK low time	100	—	ns
tHZ	Hold time for SPI_MISO signal (transition back to high-z state)	—	15	ns
tSCS	Setup time for SPI_CS_B signal	125	—	ns
tHCS	Hold time for SPI_CS_B signal	240	—	ns
tWCS	Inactive time for SPI_CS_B signal	600	—	ns
tSET	Data setup time for SPI_MOSI signal	10	—	ns
tHOLD	Data hold time for SPI_MOSI signal	10	—	ns
tDDLY	Setup time for SPI_MISO signal (transition out of high-z state)	—	50	ns

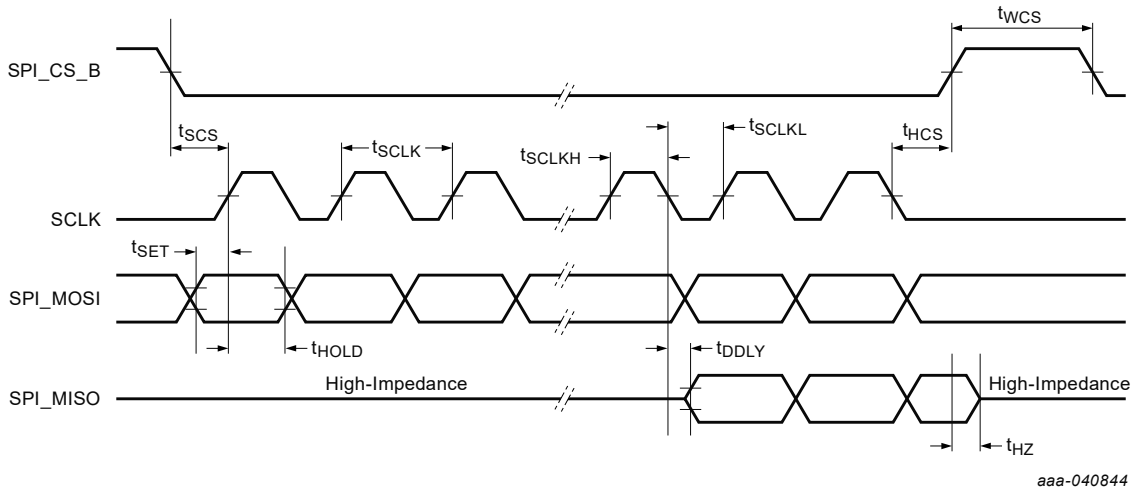


Figure 12. SPI timing diagram (4-wire mode)

13.6 SPI timing specifications (software enabled 3-wire mode)

Table 14 and Figure 13 specify and illustrate the minimum and maximum timing parameter values for correct SPI interface functionality when FXLS8967AF is operated in 3-wire (software enabled) SPI mode. FXLS8967AF only supports SPI mode '00', corresponding to CPOL = 0, and CPHA = 0. In this mode, the active state of the clock is high and the idle state is low. Data is latched on the rising edge of the clock and propagated on the falling edge. All timing specifications shown in Table 14 were determined under the following conditions: 10 pF capacitor and 1 kΩ pull-up resistor present on all SPI signals, 105 °C, 1.8 V.

Note: *When FXLS8967AF is operated in 3-wire SPI mode - by setting* ***SENS_CONFIG1[****SPI_M****]*** *= 1 - the SA0/SPI_MISO pin is always placed in a high impedance (high-z) state, with the SPI_MISO pin output driver disabled (tri-stated).*

Table 14. Secondary timing values

Label	Description	Specifications		Unit
		Min.	Max.	
fSCLK	SCLK frequency	0	4	MHz
tSCLK	SCLK Period	250	—	ns
tSCLKH	SCLK high time	100	—	ns
tSCLKL	SCLK low time	100	—	ns
tSCS	Setup time for SPI_CS_B signal	125	—	ns
tHCS	Hold time for SPI_CS_B signal	240	—	ns
tHZ	Hold time for SPI_DATA signal transition back to high-impedance state	—	25	ns
tWCS	Inactive time for SPI_CS_B signal	600	—	ns
tSET	Data setup time for SPI_DATA signal	10	—	ns
tHOLD	Data hold time for SPI_DATA signal	10	—	ns
tDDLY	Data setup time for SPI_DATA signal (output phase)	—	50	ns

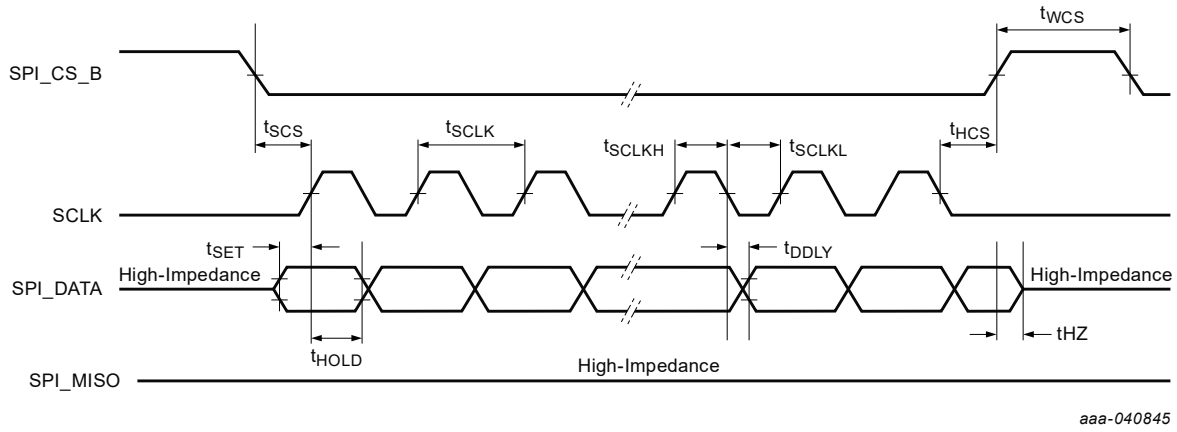


Figure 13. SPI timing diagram (3-wire mode)

14 Operating modes

Table 15. FXLS8967AF operating modes descriptions

Mode[1]	I^2C/SPI bus state	V_{DD}	Description
OFF	Unavailable	< 1.71 V	Communication with FXLS8967AF is not possible, but communications with other devices on the same I^2C/SPI bus is possible provided the V_{DD} supply pin is left floating/unconnected and not connected to GND. If V_{DD} is not left floating/unconnected, the ESD protection diodes on the interface pins could become forward biased and clamp the bus, preventing normal operation. As soon as the supply reaches 1.71 V, the device BOOT process begins.
BOOT	Unavailable	≥ 1.71 V	**BT_MODE = GND:** In this phase, the device is initialized and any default configuration parameters are loaded from OTP memory. When this phase is complete, the SRC_BOOT bit is set and a $T_{PULSE-BOOT1}$ µs pulse may be signaled on either one of the INT1/2 pins (defaults enabled on the INT1 pin after POR). **BT_MODE = V_{DD}:** In this phase, the device is initialized and any default configuration parameters are loaded from OTP memory, along with any default Motion Detection function specific parameters. When the default configuration parameters are loaded from OTP memory, the SRC_BOOT bit is set and a boot pulse, $T_{PULSE-BOOT2}$, can be signaled on the INT2 pin. By default, the boot pulse is routed to INT2 pin and cannot be routed to INT1 pin.

Table 15. FXLS8967AF operating modes descriptions...*continued*

Mode[1]	I^2C/SPI bus state	V_{DD}	Description
Hibernate[2]	Unavailable	≥ 1.71 V	The wake-up detection circuit is active, but all other analog and digital blocks are disabled to minimize the current drawn on the V_{DD} pin. I^2C and SPI interfaces are not available, and all previously written register settings are lost. **BT_MODE = GND:** The host must toggle the SPI_CS_B / WAKE-UP pin (low-to-high or high-to-low) in order to initiate a transition back into Standby mode before attempting communications with the device. The host must wait T_{BOOT1} ms for the boot process to complete. **BT_MODE = V_{DD}:** The INT1/MOT_DET pin is set high (level sensitive) through an external pull-up resistor; the device then exits Hibernate mode and starts the BOOT process. The host must wait T_{BOOT2} ms for the boot process to complete and the motion detection process to begin. Communication with the device over the I2C or SPI interfaces is possible after the BOOT process completes.
Standby	Available	≥ 1.71 V	Sensor and analog blocks are disabled; I^2C and SPI interfaces are available.
Active[3][4] (WAKE/ SLEEP)	Available	≥ 1.71 V	Sensor and analog blocks are enabled when needed (power cycled). I^2C and SPI interfaces are available. **BT_MODE = GND:** FXLS8967AF can automatically transition between the Active SLEEP and WAKE sub-modes when activity/inactivity is detected. Setting **ASLP_COUNT** ≥ 1 enables the Auto-WAKE/SLEEP mode. **BT_MODE = V_{DD}:** The Auto-WAKE/SLEEP function is not typically used in this mode (defaults to disabled), but the host may enable Auto-WAKE/SLEEP by configuring it through the register interface.
Active[5] (EXT_TRIG)	Available	≥ 1.71 V	All blocks are enabled when needed (power cycled). I^2C and SPI interfaces are able to respond to read and write commands. **BT_MODE = GND:** **SENS_CONFIG4[**INT2_FUNC**]** = 1 FXLS8967AF automatically transitions between EXT_TRIG and Active mode upon receiving a trigger signal (low-to-high transition) on the EXT_TRIG/INT2 pin. Once the measurement cycle has completed, FXLS8967AF automatically transitions back to the EXT_TRIG state and waits for the next trigger event. **BT_MODE = V_{DD}:** External trigger mode is not available; **SENS_CONFIG4 [**INT2_FUNC**]** shall not be written to with any value other than 0.

[1] All register contents are preserved when transitioning from Active to Standby mode. Some registers are reset when transitioning from Standby to Active. The behavior of all registers is noted in Table 20.

[2] Exiting Hibernate mode causes all register settings to initialize to their default values. Entering Hibernate mode is equivalent to removing the V_{DD} supply; the device state, sensor data, and host programmed register contents are lost when this mode is entered.

[3] The SLEEP and WAKE modes are Active measurement modes. For more information on how to use the SLEEP and WAKE modes and how to transition between these modes, see Table 16.

[4] The SLEEP and WAKE modes each feature independent power mode and ODR settings for the HPM and LPM modes. FPM may also be independently enabled for either WAKE or SLEEP modes, allowing for user programmable idle times and measurement decimation factors. These features allow for the creation of custom ODRs and also realizing the optimal trade-off between resolution (noise) and power dissipation in a given application or use case.

[5] The EXT_TRIG mode may be used to synchronize the collection of acceleration and temperature data with an external system, or to create custom ODRs using an MCU output compare/PWM/GPIO pin.

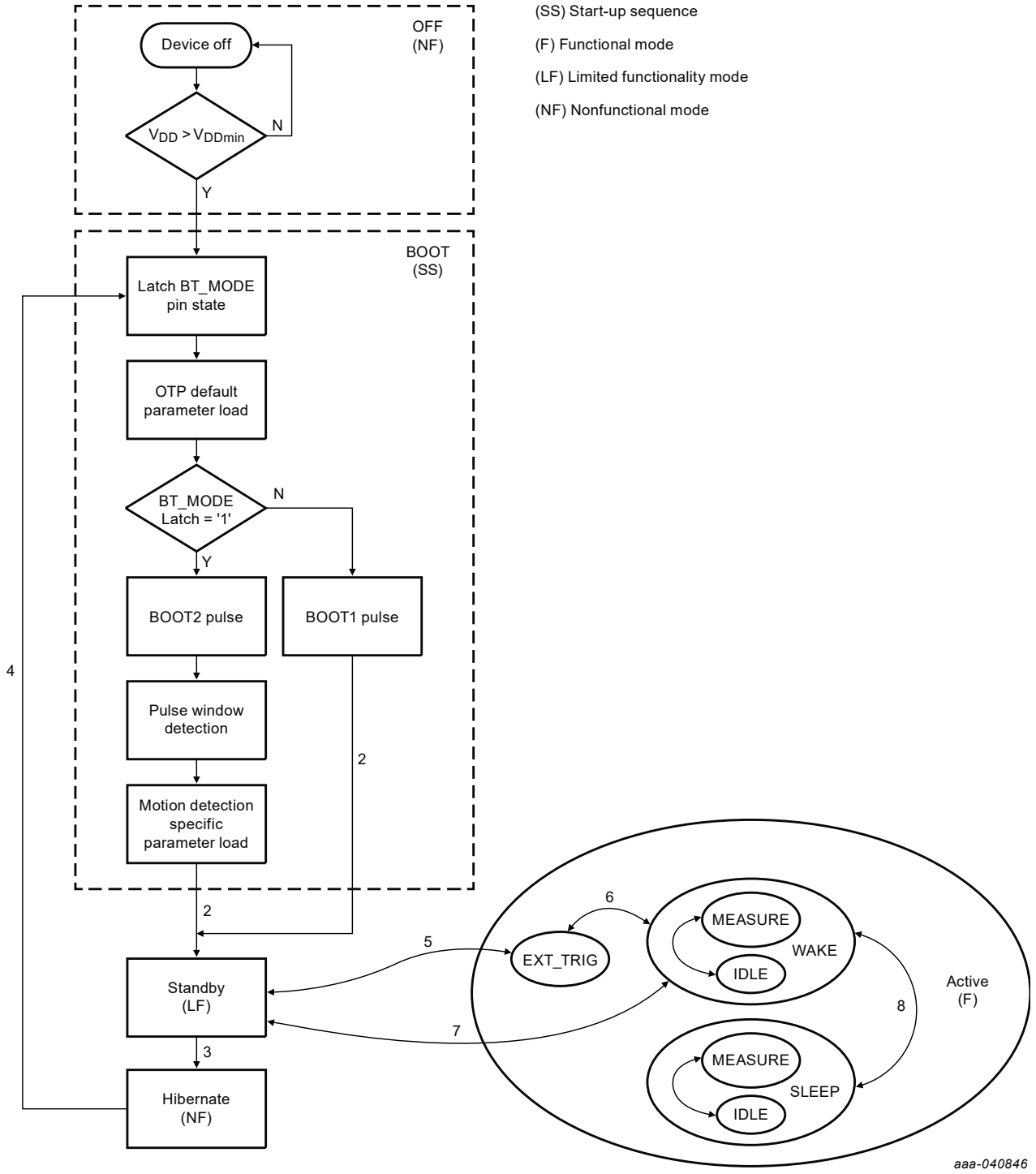


Figure 14. Operating modes transition diagram

Table 16. Operating modes transition criteria

Callout	Current mode	Next mode	Transition criteria
1	OFF	BOOT	Apply $V_{DD} \geq V_{DD}min$
2	BOOT	Standby	**BOOT_MODE = GND:** Wait T_{BOOT1} ms after applying $V_{DD} \geq VDD_{min}$; FXLS8967AF enters Standby mode and waits for I^2C/SPI commands. **BT_MODE = V_{DD}:** Wait T_{BOOT2} ms after setting the INT1 / MOT_DET pin high. FXLS8967AF automatically transitions into WAKE (**SENS_CONFIG1[**ACTIVE**]** bit is automatically set, see callout 7).
3	Standby	Hibernate	**BOOT_MODE = GND:** Set **SENS_CONFIG5[**HIBERNATE_EN**]** = 1; the device may then be woken up only by toggling the SPI_CS_B / WAKE_UP pin. **BOOT_MODE = V_{DD}:** The host MCU drives the MOT_DET pin low for ≥ $T_{MOT-HIB}$ ms to enter Hibernate mode. The device remains in Hibernate mode as long as the MOT_DET pin remains low.[1]
4	Hibernate	BOOT	**BT_MODE = GND:** The host MCU must toggle the SPI_CS_B / WAKE_UP pin **BT_MODE = V_{DD}:** FXLS8967AF exits Hibernate mode and begins the BOOT sequence when the MOT_DET pin is pulled high.
5	Standby	EXT_TRIG	**BT_MODE = GND:** Enable the EXT_TRIG input function by setting **SENS_CONFIG4[**INT2_FUNC**]** = 1. **BT_MODE = V_{DD}:** The EXT_TRIG function is not available when BT_MODE = V_{DD}; this transition is not possible
	EXT_TRIG	Standby	**BT_MODE = GND:** Disable the EXT_TRIG input function by setting **SENS_CONFIG4[**INT2_FUNC**]** = 0. **BT_MODE = V_{DD}:** The EXT_TRIG function is not available when BT_MODE = V_{DD}; this transition is not possible
6	EXT_TRIG	WAKE	**BT_MODE = GND:** To initiate an ADC conversion, signal a low to high state transition on the INT2/ EXT_TRIG pin. **BT_MODE = V_{DD}:** The EXT_TRIG function is not available when BT_MODE = V_{DD}; this transition is not possible
	WAKE	EXT_TRIG	**BT_MODE = GND:** FXLS8967AF automatically returns to the EXT_TRIG state once the previously triggered measurement has completed. **BT_MODE = V_{DD}:** The EXT_TRIG function is not available when BT_MODE = V_{DD}; this transition is not possible

Table 16. Operating modes transition criteria*...continued*

Callout	Current mode	Next mode	Transition criteria
7	Standby	WAKE	**BT_MODE = GND:** Set **SENS_CONFIG1[**ACTIVE**]** = 1 **BT_MODE = V_{DD}:** The **SENS_CONFIG1[**ACTIVE**]** bit is set automatically after the BOOT process completes when the INT1/MOT_DET pin is held high. The host may also manually set this bit using the I^2C or SPI interfaces to resume motion detection mode after changing the device configuration (after entering Standby mode from WAKE mode via register command)
	WAKE	Standby	**BT_MODE = GND:** Set **SENS_CONFIG1[**ACTIVE**]** = 0 **BT_MODE = V_{DD}:** The **SENS_CONFIG1[**ACTIVE**]** bit clears automatically when the INT1/MOT_DET pin is brought low for ≥ T_{MOT_HIB} ms; The host may also manually clear this bit using the I^2C or SPI interfaces in order to change the default device configuration.
8	WAKE	SLEEP	When **ASLP_CNT** ≥ 1, the device transitions to the SLEEP mode when none of the configured AWS interrupt sources clear the Auto-Wake/Sleep timer before it expires (host programmed **ASLP_CNT** value is reached), allowing the device to conserve energy by automatically using a lower ODR and/or power (performance) mode.
	SLEEP	WAKE	One or more of the configured AWS event sources triggers the exit from SLEEP mode and entry into WAKE.

[1] The host may also set **SENS_CONFIG5[**HIBERNATE_EN**]** = 1 to enter Hibernate mode, but a logic state transition on the SPI_CS_B / WAKE_UP pin does not cause the device to exit Hibernate mode when BT_MODE = V_{DD}.

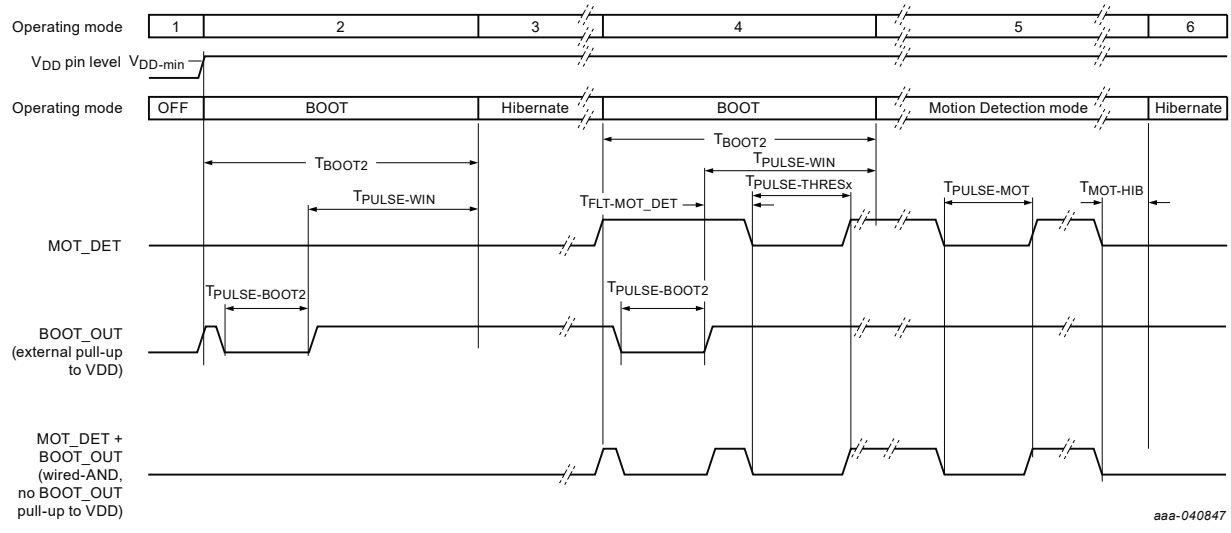


Figure 15. BOOT2 sequence and One-wire motion-detection protocol diagram (BT_MODE = V_{DD})

Table 17. BOOT2 sequence and One-wire motion protocol phase descriptions

Protocol phase	Description
1	V_{DD} supply is not present (V_{DD} < VDD_{min}); MCU and FXLS8967AF are both OFF; all IO pins are floating/high-z.
2	V_{DD} ≥ VDD_{min}; MCU and FXLS8967AF are turned on; FXLS8967AF performs the BOOT sequence. During this phase, the MOT_DET input and BOOT_OUT open-drain output functions are enabled. FXLS8967AF turns on the BOOT_OUT output for $T_{PULSE-BOOT2}$ ms. ***Note:*** *The BOOT_OUT pulse is not observable in the wired-AND configuration as it is assumed the host MCU has not yet enabled the pull-up resistor on the MOT_DET and BOOT_OUT pins (one pull-up resistor for both pins).*
3	If the MCU has not yet asserted the MOT_DET pin, FXLS8967AF enters Hibernate mode directly after the BOOT sequence. During this phase, FXLS8967AF MOT_DET pin input function remains enabled, waiting for the MOT_DET pin to go high, which triggers an exit from this mode.
4	The MCU asserts the MOT_DET pin high by enabling the pull-up; FXLS8967AF exits Hibernate mode and performs the BOOT sequence. Anytime within $T_{PULSE-WIN}$ ms after the BOOT_OUT pulse rising edge (measured from the VOL point), the host MCU may pulse the MOT_DET line low to signal the desired motion detection threshold selection. If no pulse is seen within this window, the default $T_{PULSE-THRES0}$ threshold value is used. The available pulse selections are shown in Table 18. The pulse is only recognized if it begins and ends within the $T_{PULSE-WIN}$ ms period after the BOOT_OUT pulse rising edge, and also conforms to the min and max values as shown in Table 18. If an invalid pulse width is observed, it is ignored and the default threshold value used instead.
5	Motion detection phase: FXLS8967AF continually scans for motion at the preconfigured ODR. If the motion threshold and debounce criteria are met, a $T_{PULSE-MOT}$ ms pulse is signaled on the MOT_DET pin (Open-Drain output is turned on). During this phase, the host may also communicate with FXLS8967AF over the I^2C or SPI interfaces.
6	Hibernate mode: When motion detection is no longer needed, the host MCU drives MOT_DET low forcing FXLS8967AF into Hibernate mode to conserve power. FXLS8967AF delays the entry into Hibernate mode for $T_{MOT-HIB}$ ms after the MOT_DET pin is brought low to debounce the line.

Table 18. One-wire motion protocol threshold selections

Selection	Min pulse (µs)	Nom pulse (µs)	Max pulse (µs)	Upper threshold counts (mg)[1]	Lower threshold counts (mg)[1]
$T_{PULSE-THRES0}$ (default)	—	0	—	64 (125)	–64 (–125)
$T_{PULSE-THRES1}$	562.5	625	883	32 (62)	–32 (–62)
$T_{PULSE-THRES2}$	1125	1250	1570	96 (187)	–96 (–187)
$T_{PULSE-THRES3}$	2250	2500	2950	128 (250)	–128 (–250)

[1] Threshold m*g* values assume the default ±4 *g* FSR is used (sensitivity of 1.95 m*g*/LSB, typical)

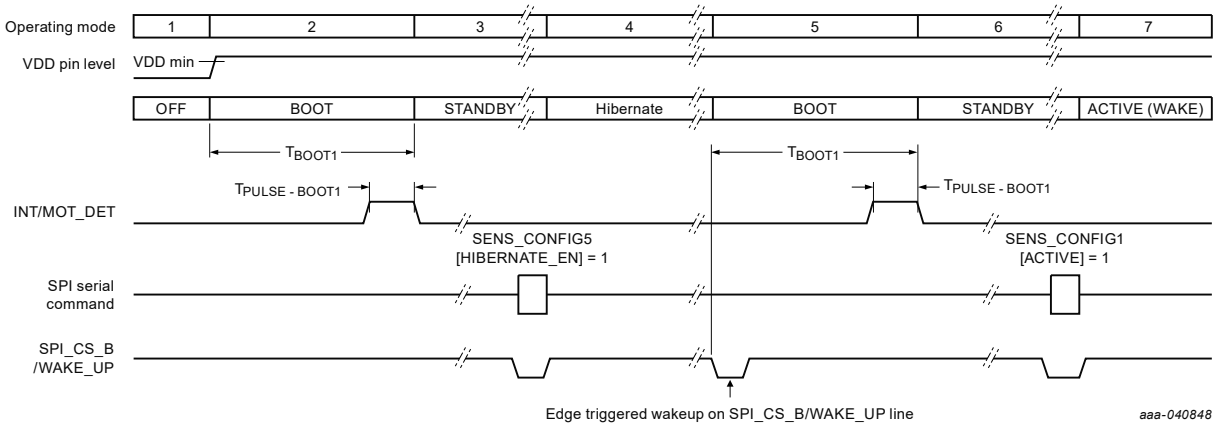


Figure 16. BOOT1 sequence (BT_MODE = GND)

Table 19. BOOT1 sequence description (BT_MODE = GND)

Protocol phase	Description
1	V_{DD} supply is not present (V_{DD} < VDD_{min}); MCU and FXLS8967AF are both off; all IO pins are floating/high-z.
2	V_{DD} ≥ VDD_{min}; MCU and FXLS8967AF are turned on; FXLS8967AF performs the BOOT sequence and provides the BOOT_OUT output pulse for $T_{PULSE-BOOT1}$ ms.
3	FXLS8967AF enters standby mode directly after the BOOT sequence.
4	When the MCU sends a serial command to set **SENS_CONFIG5[**HIBERNATE_EN**]** bit to 1, FXLS8967AF enters Hibernate mode. NOTE: The device enters into Hibernate mode 1us (typ) after the SPI_CS_B line is de-asserted for the corresponding HIBERNATE_EN serial command.
5	To wake up the device from Hibernate mode, the MCU toggles the SPI_CS_B/WAKE UP pin (see $T_{FLT-WAKE\_UP}$ deglitch filter time for transition out of Hibernate mode); FXLS8967AF performs the BOOT sequence and provides the BOOT_OUT output pulse for $T_{PULSE-BOOT1}$ ms.
6	FXLS8967AF enters standby mode directly after the BOOT sequence.
7	When the MCU sends a serial command to set **SENS_ CONFIG1[**ACTIVE**]** bit to 1, FXLS8967AF enters active mode.

15 Register descriptions

Table 20. Register address map

Name	Type	Register Address	Auto-increment Address		Default Values BT_MODE = GND/[V_{DD}]	Comment
			F_READ = 0	F_READ = 1		
INT_STATUS [1] [2]	R	00h	01h/02h/04h/06h/ 08h/0Ch/0Eh/10h		01h	Interrupt and system status event flags.
TEMP_OUT [1]	R	01h	02h/04h/06h/08h/ 0Ch/0Eh/10h		—	Temperature output data – temp_out[7:0]. When **SENS_CONFIG2[**AINC_TEMP**]** = 0 the auto-increment mechanism skips this register.
VECM_LSB [1] [3]	R	02h	03h	04h/06h/08h/ 0Ch/0Eh/10h	—	12-bit unsigned vector magnitude LSB/MSB: VECM[7:0] (LSB) when **SENS_CONFIG2[**LE_BE**]** = 0, and VECM[11:4] (MSB) when **SENS_ CONFIG2[**LE_BE**]** = 1. This register is skipped over by the auto-increment mechanism when **SENS_ CONFIG5[**VECM_EN**]** = 0.

Table 20. Register address map...*continued*

Name	Type	Register Address	Auto-increment Address		Default Values BT_MODE = GND/[V_{DD}]	Comment
			F_READ = 0	F_READ = 1		
VECM_MSB [1] [3]	R	03h	04h/06h/08h/0Ch/0Eh/10h		—	12-bit unsigned vector magnitude MSB/LSB: VECM[11:8] (MSB) when **SENS_CONFIG2[**LE_BE**]** = 0, and VECM[3:0] (LSB) when **SENS_CONFIG2[**LE_BE**]** = 1. This register is skipped over by the auto-increment mechanism when **SENS_CONFIG5[**VECM_EN**]** = 0.
OUT_X_LSB [1] [3]	R	04h	05h	06h/08h/00h	—	LSB/MSB of current 12-bit X-axis accelerometer output data – x_data_out[7:0] when **SENS_CONFIG2[**LE_BE**]** = 0 and x_data_out[11:4] when **SENS_CONFIG2[**LE_BE**]** = 1. When **SENS_CONFIG5[**X_DIS**]** = 1, this register is skipped over by the auto-increment mechanism.
OUT_X_MSB [1] [3]	R	05h	06h/08h/00h		—	MSB/LSB of current 12-bit X-axis accelerometer output data – x_data_out[11:8] when **SENS_CONFIG2[**LE_BE**]** = 0 and x_data_out[3:0] when **SENS_CONFIG2[**LE_BE**]** = 1. When **SENS_CONFIG5[**X_DIS**]** = 1, this register is skipped over by the auto-increment mechanism.
OUT_Y_LSB [1] [3]	R	06h	07h	08h/00h	—	LSB/MSB of current 12-bit Y-axis accelerometer output data – y_data_out[7:0] when **SENS_CONFIG2[**LE_BE**]** = 0 and y_data_out[11:4] when **SENS_CONFIG2[**LE_BE**]** = 1. When **SENS_CONFIG5[**Y_DIS**]** = 1, this register is skipped over by the auto-increment mechanism.
OUT_Y_MSB [1] [3]	R	07h	08h/00h		—	MSB/LSB of current 12-bit Y-axis accelerometer output data – y_data_out[11:8] when **SENS_CONFIG2[**LE_BE**]** = 0 and y_data_out[3:0] when **SENS_CONFIG2[**LE_BE**]** = 1. When **SENS_CONFIG5[**Y_DIS**]** = 1, this register is skipped over by the auto-increment mechanism.
OUT_Z_LSB [1] [3]	R	08h	09h	00h	—	LSB/MSB of current 12-bit Z-axis accelerometer output data – z_data_out[7:0] when **SENS_CONFIG5[**LE_BE**]** = 0 and z_data_out[11:4] when **SENS_CONFIG2[**LE_BE**]** = 1. When **SENS_CONFIG5[**Z_DIS**]** = 1, this register is skipped over by the auto-increment mechanism.
OUT_Z_MSB [1] [3]	R	09h	00h		—	MSB/LSB of current 12-bit Z-axis accelerometer output data – z_data_out[11:8] when **SENS_CONFIG2[**LE_BE**]** = 0 and z_data_out[3:0] when **SENS_CONFIG2[**LE_BE**]** = 1. When **SENS_CONFIG5[**Z_DIS**]** = 1, this register is skipped over by the auto-increment mechanism.
Reserved registers						
RESERVED_REG1	—	0Ah	0Bh		00h	Factory reserved register address 1
Output Buffer Configuration and Status						
BUF_STATUS [1][2]	R	0Bh	0Ch/0Eh/10h		00h	Buffer watermark and overflow status flags; stored sample count (buf_cnt[5:0])
BUF_X_LSB [1][3][4]	R	0Ch	0Dh	0Eh/10h/0Ch	—	Head/Tail sample of output buffer X-axis LSB - buf_x_out[7:0] when **SENS_CONFIG2[**LE_BE**]** = 0 and buf_x_out[11:4] when **SENS_CONFIG2[**LE_BE**]** = 1. When **SENS_CONFIG5[**X_DIS**]** = 1, this register is skipped over by the auto-increment mechanism.
BUF_X_MSB [1][3][4]	R	0Dh	0Eh/10h/0Ch		—	Head/Tail sample of output buffer X-axis MSB - buf_x_out[11:8] when **SENS_CONFIG2[**LE_BE**]** = 0 and buf_x_out[3:0] when **SENS_CONFIG2[**LE_BE**]** = 1. When **SENS_CONFIG5[**X_DIS**]** = 1, this register is skipped over by the auto-increment mechanism.

Table 20. Register address map...*continued*

Name	Type	Register Address	Auto-increment Address		Default Values BT_MODE = GND/[V_{DD}]	Comment
			F_READ = 0	F_READ = 1		
BUF_Y_LSB[1][3][4]	R	0Eh	0Fh	10h/0Ch/0Eh	—	Head/Tail sample of output buffer Y-axis LSB - buf_y_out[7:0] when **SENS_CONFIG2[**LE_BE**]** = 0 and buf_y_out[11:4] when **SENS_CONFIG2[** LE_BE**]** = 1. When **SENS_CONFIG5[**Y_DIS**]** = 1, this register is skipped over by the auto-increment mechanism.
BUF_Y_MSB[1][3][4]	R	0Fh	10h/0Ch/0Eh		—	Head/Tail sample of output buffer Y-axis MSB - buf_Y_out[11:8] when **SENS_CONFIG2[**LE_BE**]** = 0 and buf_y_out[3:0] when **SENS_CONFIG2[**LE_BE**]** = 1. When **SENS_CONFIG5[**Y_DIS**]** = 1, this register is skipped over by the auto-increment mechanism.
BUF_Z_LSB[1][3][4]	R	10h	11h	0Ch/0Eh/10h	—	Head/Tail sample of output buffer Z-axis LSB - buf_z_out[7:0] when **SENS_CONFIG2[**LE_BE**]** = 0 and buf_z_out[11:4] when **SENS_CONFIG2[**LE_BE**]** = 1. When **SENS_CONFIG5[**Z_DIS**]** = 1, this register is skipped over by the auto-increment mechanism.
BUF_Z_MSB[1][3][4]	R	11h	0Ch/0Eh/10h		—	Head/Tail sample of output buffer Z-axis MSB - buf_Z_out[11:8] when **SENS_CONFIG2[**LE_BE**]** = 0 and buf_z_out[3:0] when **SENS_CONFIG2[**LE_BE**]** = 1. When **SENS_CONFIG5[**Z_DIS**]** = 1, this register is skipped over by the auto-increment mechanism.
Device identification						
PROD_REV	R	12h	13h		13h	Product revision number in BCD format [maj.min] with range 1.0 to 9.9
WHO_AM_I[1]	R	13h	14h		87h	8-bit NXP unique sensor product ID.
System status register						
SYS_MODE [1] [2]	R	14h	15h		00h/[01h]	Current system operating mode, buffer gate error flag, and buffer gate error sample count
Device configuration and control registers						
SENS_CONFIG1 [1] [5]	R/W	15h	16h		00h/[03h]	Full-scale range selection, self-test axis, and polarity selection, soft reset, Active mode enable.
SENS_CONFIG2 [1] [5]	R/W	16h	17h		00h	WAKE and SLEEP power mode selections, little/big endian output mode, auto-increment control, fast read enable.
SENS_CONFIG3 [1] [5]	R/W	17h	18h		00h/[C0h]	WAKE and SLEEP mode ODR and decimation selections
SENS_CONFIG4 [1] [5]	R/W	18h	19h		01h	Auto-WAKE/SLEEP interrupt source enable bits, interrupt output pin logic polarity, and driver type, external trigger input function enable
SENS_CONFIG5 [1] [5]	R/W	19h	1Ah		00h/[00h]	Auto-increment mechanism disable bits for X/Y/Z axis data; Hibernate mode enable
WAKE_IDLE_LSB [1] [5]	R/W	1Ah	1Bh		00h	LSB of 12-bit user programmable WAKE mode idle time - wake_idle[7:0]
WAKE_IDLE_MSB [1] [5]	R/W	1Bh	1Ch		00h	MSB of 12-bit user programmable WAKE mode idle time - wake_idle[11:8]
SLEEP_IDLE_LSB [1] [5]	R/W	1Ch	1Dh		00h	LSB of 12-bit user programmable SLEEP mode idle time - sleep_idle[7:0]
SLEEP_IDLE_MSB [1] [5]	R/W	1Dh	1Eh		00h	MSB of 12-bit user programmable SLEEP mode idle time - sleep_idle[11:8]
ASLP_COUNT_LSB [1] [5]	R/W	1Eh	1Fh		00h	LSB of inactivity time-out count value used for transitioning into Auto-SLEEP mode: aslp_count[7:0]. In order to enable the Auto-WAKE/SLEEP feature, the value written to this register must be ≥ 1.
ASLP_COUNT_MSB [1] [5]	R/W	1Fh	20h		00h	MSB of inactivity time-out count value used for transitioning into Auto-SLEEP mode: aslp_count[11:8]

Table 20. Register address map...*continued*

Name	Type	Register Address	Auto-increment Address		Default Values BT_MODE = GND/[V_{DD}]	Comment
			F_READ = 0	F_READ = 1		
INT_EN [1] [5]	R/W	20h	21h		00h/[20h]	Interrupt output enable register
INT_PIN_SEL [1] [5]	R/W	21h	22h		00h	Interrupt output routing register (INT1, INT2 pins)
Zero-*g* offset compensation registers						
OFF_X [1] [5]	R/W	22h	23h		00h	X-Axis acceleration zero-*g* offset: x_off[7:0]
OFF_Y [1] [5]	R/W	23h	24h		00h	Y-Axis acceleration zero-*g* offset: y_off[7:0]
OFF_Z [1] [5]	R/W	24h	25h		00h	Z-Axis acceleration zero-*g* offset: z_off[7:0]
Output Buffer Configuration						
RESERVED_REG2	—	25h	26h		00h	Factory reserved register address 2
BUF_CONFIG1 [1] [5]	R/W	26h	27h		00h	Output data buffer operating mode, trigger source selection, and data collection mode.
BUF_CONFIG2 [1] [5]	R/W	27h	28h		00h	Output data buffer flush, gate control, and watermark level (buf_wmrk[5:0]). **The BUF_FLUSH bit may be set at any time in either STANDBY, ACTIVE, OR EXT_TRIG modes.*
Orientation detection function configuration and status						
ORIENT_STATUS [1] [2]	R	28h	29h		00h	Orientation event status
ORIENT_CONFIG [1] [5]	R/W	29h	2Ah		80h	Orientation detection function configuration.
ORIENT_DBCOUNT [1] [5]	R/W	2Ah	2Bh		00h	Orientation detection change debounce counter
ORIENT_BF_ZCOMP [1] [5]	R/W	2Bh	2Ch		44h	Back/Front orientation state change threshold angle.
ORIENT_THS_REG [1] [5]	R/W	2Ch	2Dh		84h	Orientation detection state change threshold angle (Portrait/Landscape) and hysteresis settings.
Sensor data change detection function configuration and status						
SDCD_INT_SRC1 [1] [2]	R	2Dh	2Eh		00h	Sensor Data Change Detection function outside-of-thresholds event flags source register.
SDCD_INT_SRC2 [1] [2]	R	2Eh	2Fh		00h	Sensor Data Change Detection function within thresholds event flags source register.
SDCD_CONFIG1 [1] [5]	R/W	2Fh	30h		00h/[38h]	Sensor Data Change Detection function configuration register 1 – Enables event latch and individual axis bits for OT and WT logic function functions.
SDCD_CONFIG2 [1] [5]	R/W	30h	31h		00h/[D8h]	Sensor Data Change Detection function configuration register 2 – SDCD function enable, reference values initialization, and update behavior, relative/absolute operating mode selection, debounce counter behavior. ***Note:*** *Only the REF_UPD bit may be set in Active mode.*
SDCD_OT_DBCNT [1] [5]	R/W	31h	32h		00h/[00h]	Sensor Data Change Detection outside of thresholds condition debounce count value sdcd_ot_dbcnt[7:0]
SDCD_WT_DBCNT [1] [5]	R/W	32h	33h		00h/[00h]	Sensor Data Change Detection within thresholds condition debounce count value – sdcd_wt_dbcnt[7:0]
SDCD_LTHS_LSB [1] [5]	R/W	33h	34h		00h/[C0h]	Sensor Data Change Detection lower threshold value LSB - sdcd_lths[7:0]
SDCD_LTHS_MSB [1] [5]	R/W	34h	35h		00h/[0Fh]	Sensor Data Change Detection lower threshold value MSB - sdcd_lths[11:8].
SDCD_UTHS_LSB [1] [5]	R/W	35h	36h		00h/[40h]	Sensor Data Change Detection upper threshold value LSB - sdcd_uths[7:0]
SDCD_UTHS_MSB [1] [5]	R/W	36h	37h		00h/[00h]	Sensor Data Change Detection upper threshold value MSB - sdcd_uths[11:8]
SELF_TEST_CONFIG1 [1] [5]	R/W	37h	38h		00h	Self-Test Idle phase duration:
SELF_TEST_CONFIG2 [1] [5]	R/W	38h	39h		00h	Self-Test measurement phase decimation factor

Table 20. Register address map...*continued*

Name	Type	Register Address	Auto-increment Address		Default Values BT_MODE = GND/[V_{DD}]	Comment
			F_READ = 0	F_READ = 1		
reserved register 12	R/W	39h	3Ah		00h	Factory reserved register; do not modify
reserved register 13[1]	R	3Ah	00h		—	Factory reserved register

[1] Register contents are preserved when a transition from ACTIVE to STANDBY mode occurs. All register contents are lost when a transition from Hibernate mode or a POR/BOR event occurs.
[2] Register contents are reset when a transition from STANDBY to ACTIVE or EXT_TRIG mode occurs.
[3] The byte order and L/R justification of these registers is user programmable between little-endian right justified and big-endian (left justified) modes. The default mode is little-endian, right justified. The byte order and justification is controlled by **SENS_CONFIG3**[LE_BE].
[4] The output data buffer contents become obsolete whenever a transition from STANDBY-to-ACTIVE or STANDBY-to-EXT_TRIG modes occurs.
[5] Register contents can only be modified while the device is in STANDBY mode; the only exceptions are the **SENS_CONFIG1[**ACTIVE**]**, **SENS_CONFIG1[**RST**]** and **BUF_CONFIG1[**BUF_FLUSH**]** bits that may be set at any time in STANDBY, ACTIVE, or EXT_TRIG modes. The ACTIVE bit state cannot be modified while in EXT_TRIG operating mode.

15.1 INT_STATUS register (address 00h)

Table 21. INT_STATUS register (address 00h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	SRC_DRDY	SRC_OVF	SRC_BUF	SRC_ SDCD_OT	SRC_ SDCD_WT	SRC_ ORIENT	SRC_ASLP	SRC_BOOT
Reset	0	0	0	0	0	0	0	1
Access	R	R	R	R	R	R	R	R

Table 22. INT_STATUS register (address 00h) bit description

Field	Description
7 SRC_DRDY	Output data-ready event flag 0: A new set of XYZ acceleration and temperature data is not available. 1: A new set of XYZ acceleration and temperature data is available ***Notes:*** • The SRC_DRDY flag is cleared whenever one or more of the VECM, and **OUT_X/Y/Z** registers are read. • Whenever **BUF_CONFIG1[**BUF_MODE1:0**]** > 00b (buffer enabled), SRC_DRDY is held at logic '0'. • When BT_MODE=GND, SRC_DRDY bit and the signaled interrupt are cleared whenever one or more of the VECM, and OUT_X/Y/Z registers are read. • When BT_MODE=V_{DD}, SRC_DRDY bit is cleared whenever one or more of the VECM, and OUT_X/Y/Z registers are read. However the data ready interrupt is signaled for $T_{PULSE-MOT}$ seconds (5 ms typ) and it clears itself automatically. The current data ready interrupt pulse is terminated when the device transitions into STANDBY mode before its completion and therefore may not span for entire $T_{PULSE-MOT}$ seconds.
6 SRC_OVF	Output data overflow event flag 0: No overflow condition detected. 1: A new set of XYZ acceleration and temperature output data latches into **OUT_X/Y/Z** and **TEMP_OUT** registers before the previous set is completely read by the host. ***Notes:*** • *SRC_OVF is not set if at least one of the **OUT_X/Y/Z** registers was read before the new data set arrives.* • *Whenever the **INT_STATUS** register is read, SRC_OVF is cleared.* • *Whenever **BUF_CONFIG1[BUF_MODE[**1:0**]]** > 00b (buffer enabled), SRC_OVF is held at logic '0'.*

Table 22. INT_STATUS register (address 00h) bit description*...continued*

Field	Description
5 SRC_BUF	Output data buffer status event flag 0: No output buffer event status flags are active 1: One or more output buffer status event flags are active (BUF_WMRK | BUF_OVF | BUF_GATE_ERR); reading the **BUF_STATUS** register provides more information on the BUF_WMRK or BUF_OVF event flags that are currently active. Reading the **SYS_MODE** register provides information on the BUF_GATE_ERR flag status. ***Notes:*** • *The SRC_BUF flag is only active when **BUF_CONFIG1[**BUF_MODE[1:0]**]** > 00b.* • *The BUF_WMRK event flag will not participate in SRC_BUF interrupt generation in triggered mode (the BUF_WMRK flag is asserted after the buffer is triggered, but it will not signal an external interrupt as with the other buffer operating modes). If it is required to know when the trigger event has taken place, the host may use the SDCD or ORIENT interrupts, as appropriate, to indicate when the buffer is triggered. When the buffer is full, the SRC_BUF flag is set and an external interrupt is signaled on the INT1 or INT2 pins, if configured.*
4 SRC_SDCD_OT	SDCD outside of thresholds condition event flag (copy of **SDCD_INT_SRC1[**OT_EA**]** flag) 0: SDCD outside of thresholds event is not detected (**SDCD_INT_SRC1[**OT_EA**]** = 0). 1: SDCD outside of thresholds event is detected (**SDCD_INT_SRC1[**OT_EA**]** = 1). The SRC_SDCD_OT event flag is cleared by reading the **SDCD_INT_SRC1** register when **SDCD_CONFIG1[**OT_ELE**]** = 1, otherwise this flag is cleared automatically by the function when the event condition becomes false.
3 SRC_SDCD_WT	SDCD within thresholds condition event flag (copy of **SDCD_INT_SRC2[**WT_EA**]** flag) 0: No SDCD within thresholds event has been detected (**SDCD_INT_SRC2[**WT_EA**]** = 0). 1: An SDCD within thresholds event has been detected (**SDCD_INT_SRC2[**WT_EA**]** = 1). The SRC_SDCD_WT event flag is cleared by reading the **SDCD_INT_SRC2** register when **SDCD_CONFIG1[**WT_ELE**]** = 1, otherwise the function clears this flag automatically when the event condition becomes false.
2 SRC_ORIENT	Orientation change event flag The SRC_ORIENT flag is asserted whenever the **ORIENT_STATUS[**NEW_ORIENT**]** bit is asserted and a change in orientation has been detected. Reading the **ORIENT_STATUS** register clears this event flag. 0: An orientation change event has not occurred 1: An orientation change event has occurred.

Table 22. INT_STATUS register (address 00h) bit description*...continued*

Field	Description
1 SRC_ASLP	Auto-WAKE/SLEEP event status flag 0: A WAKE-to-SLEEP or SLEEP-to-WAKE system operating mode transition has not occurred. 1: A WAKE-to-SLEEP or a SLEEP-to-WAKE system operating mode transition has occurred. Reading the **SYS_MODE** register allows the host processor to determine if the transition direction was from WAKE-to-SLEEP or SLEEP-to-WAKE: • A **WAKE-to-SLEEP** transition is observed when no configured interrupt event occurs for a time period (number of ODR periods) that equals the user-specified inactivity time limit programmed in the **ASLP_COUNT_LSB** and **ASLP_COUNT_MSB** registers. On expiry of configured time period with no user specified activity, the system transitions to the user-specified SLEEP power mode (**SENS_CONFIG2[**sleep_pm**]**) and ODR (or decimation and idle time settings when Flexible Performance mode is selected). • A SLEEP-to-WAKE transition occurs when a configured interrupt event flag becomes active. The interrupt event flag transitions to the user-specified WAKE power mode (**SENS_CONFIG2[**wake_pm**]**) and ODR (or decimation and idle time settings when Flexible Performance mode is selected). ***Notes:*** • *The SRC_ASLP event flag is cleared by reading the **SYS_MODE** register.* • *The SRC_ASLP event flag is enabled when **ASLP_COUNT** ≥ 1 which also enables the Auto-WAKE/SLEEP function. The SRC_ASLP flag is only operational when **INT_EN[**ALSP_EN**]** = 1.*
0 SRC_BOOT	System boot complete event flag 0: Boot sequence in process/not complete. 1: Boot sequence completed; FXLS8967AF is now ready to accept commands over the I^2C or SPI interfaces. This flag is automatically set to 1 upon completion of the boot process and remains set until a POR, soft reset, or exit from Hibernate mode event occurs. When BT_MODE = GND: Boot interrupt is generated in INT1/MOT_DET pin by default. This event flag may be configured to generate an interrupt on either the INT1 or INT2 pin depending on the mapping selected in **INT_PIN_SEL**. When this event flag is enabled as an interrupt output, either the INT1 or INT2 (depending on the setting made in **INT_PIN_SEL** register) pin is pulsed once with a width of T_{BOOT1} µs when the boot process completes. When BT_MODE = V_{DD}: The INT2/BOOT_OUT pin is pulsed once with a duration of T_{BOOT2} ms when the boot process completes. The pulse is active low (open-drain output); an external pull-up resistor is required. ***Notes:*** • *When BT_MODE = GND, after a POR or exiting Hibernate mode, the polarity of the BOOT pulse is default Active High because any I^2C write to the **SENS_CONFIG4[**INT_POL**]** fails until the boot process has completed.* • *After a Soft Reset, the INT_POL, INT_PP_OD, and INT_PIN_SEL register settings are not reset and maintain their previous values. As a result, an I^2C or SPI write to the **SENS_CONFIG4[**(INT_PP_OD and INT_POL bits)**]** and **INT_PIN_SEL[**BOOT_INT2**]** bits before the Soft Reset determines the logic polarity, output driver type, and INT1/2 pin mapping of the subsequent Boot pulse.* • *It is not possible to observe the state of the SRC_BOOT bit at '0' over the I^2C or SPI interfaces as read and write operations fails until the boot process has completed.*

15.2 TEMP_OUT register (address 01h)

Table 23. TEMP_OUT register (address 01h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	TEMP_OUT[7:0]							
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

The **TEMP_OUT** register contains the 8-bit, 2's complement temperature value. When this register contains the value 00h, the measured temperature is 25 °C (typ). This register is updated on every ODR cycle.

15.3 VECM_LSB register (address 02h)

This register contains the LSB of the 12-bit, unsigned vector magnitude result (acceleration vector modulus); The result is only calculated when **SENS_CONFIG5[**VECM_EN**]** = 1.

Note: *Whenever the VECM_LSB or VECM_MSB registers are read the SRC_DRDY event flag is also cleared.*

The byte order of the vector magnitude output data is programmable via SENS_CONFIG2[LE_BE] and defaults to little-endian mode.

Table 24. VECM_LSB register (address 02h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	VECM[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 25. VECM_LSB register (address 02h) bit description

Field	Description
7 to 0 VECM[7:0]	LSB of the 12-bit unsigned acceleration vector modulus result

15.4 VECM_MSB register (address 03h)

This register contains the MSB of the 12-bit, unsigned vector magnitude result (acceleration vector modulus); The result is only calculated when **SENS_CONFIG5[**VECM_EN**]** = 1.

Note: *Whenever the VECM_LSB or VECM_MSB registers are read the SRC_DRDY event flag is also cleared.*

The byte order of the vector magnitude output data is programmable via **SENS_CONFIG2[**LE_BE**]** and defaults to little-endian mode.

Table 26. VECM_MSB register (address 03h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	VECM[11:8]			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 27. VECM_MSB register (address 03h) bit description

Field	Description
3 to 0 VECM[11:8]	MSB of the 12-bit unsigned acceleration vector modulus result

15.5 OUT_X_LSB, OUT_X_MSB, OUT_Y_LSB, OUT_Y_MSB, OUT_Z_LSB, OUT_Z_MSB registers (addresses 04h to 09h)

These registers contain the 12-bit X-axis, Y-axis, and Z-axis output acceleration data in 2's complement format.

The output data is latched into the **OUT_X/Y/Z** registers along with the assertion of the SRC_DRDY event flag.

When **SENS_CONFIG2[**F_READ**]** = 1, the auto-increment mechanism skips the MSB registers in a burst read transaction. This operation shortens the output data size from 6 bytes to 3 bytes per XYZ sample read.

The byte order of the output data is programmable via **SENS_CONFIG2[**LE_BE**]** and defaults to little-endian mode.

When **SENS_CONFIG2[**F_READ**]** = 1, the MSB of each axis's data is stored at the LSB address, regardless of the setting made in **SENS_CONFIG2[**LE_BE**]**.

In little-endian mode, the output data registers are arranged with the LSB of each axis's data stored at the lower address. The upper nibble (MSB) is stored at the next address, in right justified format. In little-endian mode, the MSB is sign extended to form a 16-bit 2's complement value.

In big-endian mode (**SENS_CONFIG2[**LE_BE**]** = 1), the output data registers are arranged with the MSB of each axis's data stored at the lower register address. The lower nibble is stored at the next address, and is left justified. The big-endian option allows a big-endian processor to directly read the output data into an array without the need to perform byte swaps. The host software must right shift the data by 4 bits (or divide by 16) in order to obtain the correct scaling of the output data. *The sign extension of the data must be done explicitly, depending on the C compiler used.*

Notes:

- *There is a ~40 µs delay between the ADC acquisitions of the accelerometer X,Y,Z, and temperature data. The temperature data is acquired first, followed by the X, Y, and Z axes acceleration data. All data is latched into the output registers at the same time instant, coincident with the SRC_DRDY event flag being asserted. Whenever any of the **OUT_X/Y/Z** registers is read the SRC_DRDY event flag is cleared.*
- *SX means sign extension, which is the logic level of the most significant bit of the 12-bit **OUT_X/Y/Z** register data, also known as **OUT_X/Y/Z[**11**]**.*

Table 28. OUT_X_LSB and OUT_X_MSB register (addresses 04h to 05h) with SEN_CONFIG2[LE_BE] = 0 bit allocation

Bit	7	6	5	4	3	2	1	0
Name	OUT_X[7:0]							
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
Name	SX	SX	SX	SX	OUT_X[11:8]			
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Table 29. OUT_Y_LSB and OUT_Y_MSB register (addresses 06h to 07h) with SEN_CONFIG2[LE_BE] = 0 bit allocation

Bit	7	6	5	4	3	2	1	0
Name	OUT_Y[7:0]							
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
Name	SX	SX	SX	SX	OUT_Y[11:8]			
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Table 30. OUT_Z_LSB and OUT_Z_MSB register (addresses 08h to 09h) with SEN_CONFIG2[LE_BE] = 0 bit allocation

Bit	7	6	5	4	3	2	1	0
Name	OUT_Z[7:0]							
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
Name	SX	SX	SX	SX	OUT_Z[11:8]			
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Table 31. OUT_X_LSB and OUT_X_MSB register (addresses 04h to 05h) with SEN_CONFIG2[LE_BE] = 1 bit allocation

Bit	7	6	5	4	3	2	1	0
Name	OUT_X[11:4]							
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
Name	OUT_X[3:0]				0	0	0	0
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Table 32. OUT_Y_LSB and OUT_Y_MSB register (addresses 06h to 07h) with SEN_CONFIG2[LE_BE] = 1 bit allocation

Bit	7	6	5	4	3	2	1	0
Name	OUT_Y[11:4]							
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
Name	OUT_Y[3:0]				0	0	0	0
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Table 33. OUT_Z_LSB and OUT_Z_MSB register (addresses 08h to 09h) with SEN_CONFIG2[LE_BE] = 1 bit allocation

Bit	7	6	5	4	3	2	1	0
Name	OUT_Z[11:4]							
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
Name	OUT_Z[3:0]				0	0	0	0
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

15.6 BUF_STATUS register (address 0Bh)

The content stored at this register address depends on whether the output data buffer is enabled or not. When **BUF_CONFIG1[**BUF_MODE[1:0]**]** = 00b, the output data buffer is disabled and this register always contains the value 00h.

When **BUF_CONFIG1[**BUF_MODE[1:0]**]** > 00b, the **BUF_STATUS** register content as shown in Table 34 and Table 35.

Table 34. BUF_STATUS register (address 0Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	BUF_ WMRK	BUF_OVF	BUF_CNT[5:0]					
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 35. BUF_STATUS register (address 0Bh) bit description

Field	Description
7 BUF_WMRK	Buffer Watermark Event Flag: 0: The buffer watermark level programmed in BUF_CONFIG2[BUF_WMRK[5:0]] has not been equaled or exceeded 1: The buffer watermark level programmed in BUF_CONFIG2[BUF_WMRK[5:0]] has been equaled or exceeded. This event flag may be cleared in one of the following ways: 1. The host must read out enough samples from the output buffer for **BUF_ STATUS[**BUF_CNT[5:0]**]** to go below the value set in **BUF_CONFIG2[**BUF_WMRK[5:0]**]**. 2. The host must flush the buffer by setting **BUF_CONFIG2[**BUF_FLUSH**]** = 1. 3. The host must set **BUF_CONFIG1[**BUF_MODE[1:0]**]** = 00b to disable the buffer, which also clears its contents. The watermark interrupt may be used to enable an efficient DMA-based transfer of the buffer contents to the host processor. For example, if the watermark level is set at 16 samples and the interrupt is enabled and routed to one of the INT1 or INT2 pins, the event may be used to trigger a single burst read operation of 1 (**BUF_STATUS**) + (16 samples * 2 bytes/sample * 3 (axes)) = 97 bytes to completely empty the buffer and clear the buffer status flags (when **SENS_CONFIG2[**F_READ**]** = 0), or 49 bytes when **SENS_CONFIG2[**F_READ**]** = 1. ***Note:*** *Using a DMA operation to handle the burst read operation can allow the processor to sleep or perform other tasks while the required number of samples is collected as a background activity.*
6 BUF_OVF	Buffer Overflow Event flag: 0: Buffer overflow event has not occurred. The number of samples stored in the buffer is less than or equal to 32 1: Buffer overflow event has occurred To clear this bit, the host must do one of the following: 1. At least one sample must be read in order to clear the BUF_OVF flag. 2. Flush the output buffer by setting **BUF_CONFIG2[**BUF_FLUSH**]** = 1. 3. Disable the output buffer by setting **BUF_CONFIG1[**BUF_MODE[1:0]**]** = 00b, which resets **BUF_STATUS[**BUF_CNT[5:0]**]** to zero, but does not clear the buffer contents.
5 to 0 BUF_CNT[5:0]	This field contains the count of the number of acceleration data triplets (samples) currently stored in the output data buffer (from 0-32). If the buffer is full (contains 32 samples), and an additional data triplet is received, the count remains at 32, and the BUF_OVF event flag is asserted.

15.7 BUF_X_LSB, BUF_X_MSB, BUF_Y_LSB, BUF_Y_MSB, BUF_Z_LSB, BUF_Z_MSB (addresses 0Ch to 11h)

These registers contain either the buffer Head or Tail output acceleration sample data in 2's complement format. The tail (oldest) sample is stored when the FIFO read out mode is selected, and the head (newest) sample is stored when the LIFO read out mode is selected. **BUF_CONFIG1[**BUF_TYPE**]** controls the read out mode.

The byte order of the output data is programmable via **SENS_CONFIG2[**LE_BE**]**, and defaults to little-endian mode.

In little-endian mode, the output data buffer registers are arranged with the LSB of each axes data stored at the lower address. The upper nibble (MSB) is stored at the next address, and is right justified. In little-endian mode, the buffer output data is also sign extended to avoid the need for the host software to do sign extension of the output data on a per sample (per axis) basis.

In big-endian mode (with **SENS_CONFIG2[**LE_BE**]** = 1), the output buffer data registers are arranged with the MSB of each axis data stored at the lower register address. The lower nibble(LSB) is stored at the next address, and is left justified. The lower 4 bits of the LSB are always read as '0'. The host software must right shift the data by 4 bits (or divide the value by 16) in order to obtain the correct scaling of the acceleration data.

If **SENS_CONFIG2[**F_READ**]** = 1, the auto increment mechanism skips over the MSB registers. This operation shortens the output data size from 6 bytes to 3 bytes per XYZ sample. When **SENS_CONFIG2[**F_READ**]** = 1, the MSB of each axes data is stored at the LSB address, regardless of the setting made in **SENS_CONFIG2[**LE_BE**]**. The output data size may also be reduced using the X/Y/Z_DIS bits located in the **SENS_CONFIG5** register. These bits can be used to selectively disable each axis from being read out using the auto-increment mechanism. For example, setting X_DIS causes the auto-increment mechanism to skip over the **BUF_X** LSB and MSB registers, thereby shortening the number of bytes to be read from 6 to 4, or from 3 to 2 when F_READ = 1.

Note: *Reading the **BUF_STATUS** register is not required in order to clear the BUF_WMRK event flag - if the host has mapped more than the BUF_WMRK event flag to the same interrupt pin, the **BUF_STATUS** register should be used to confirm that a BUF_WMRK event was the source of the interrupt before initiating the burst read operation.*

Table 36. BUF_X_LSB and BUF_X_MSB registers (addresses 0Ch, 0Dh) with SENS_CONFIG2[LE_BE] = 0 bit allocation

Bit	7	6	5	4	3	2	1	0
Name	BUF_X[7:0]							
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
Name	SX	SX	SX	SX	BUF_X[11:8]			
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Table 37. BUF_Y_LSB and BUF_Y_MSB registers (addresses 0Eh, 0Fh) with SENS_CONFIG2[LE_BE] = 0 bit allocation

Bit	7	6	5	4	3	2	1	0
Name	BUF_Y[7:0]							
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
Name	SX	SX	SX	SX	BUF_Y[11:8]			
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Table 38. BUF_Z_LSB and BUF_Z_MSB registers (addresses 10h, 11h) with SENS_CONFIG2[LE_BE] = 0 bit allocation

Bit	7	6	5	4	3	2	1	0
Name	BUF_Z[7:0]							
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
Name	SX	SX	SX	SX	BUF_Z[11:8]			
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Table 39. BUF_X_LSB and BUF_X_MSB registers (addresses 0Ch, 0Dh) with SENS_CONFIG2[LE_BE] = 1 bit allocation

Bit	7	6	5	4	3	2	1	0
Name	BUF_X[11:4]							
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
Name	BUF_X[3:0]				0	0	0	0
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Table 40. BUF_Y_LSB and BUF_Y_MSB registers (addresses 0Eh, 0Fh) with SENS_CONFIG2[LE_BE] = 1 bit allocation

Bit	7	6	5	4	3	2	1	0
Name	BUF_Y[11:4]							
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
Name	BUF_Y[3:0]				0	0	0	0
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Table 41. BUF_Z_LSB and BUF_Z_MSB registers (addresses 10h, 11h) with SENS_CONFIG2[LE_BE] = 1 bit allocation

Bit	7	6	5	4	3	2	1	0
Name	BUF_Z[11:4]							
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Bit	7	6	5	4	3	2	1	0
Name	BUF_Z[3:0]				0	0	0	0
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

15.8 PROD_REV register (address 12h)

The register contains the product revision number. The revision number is stored in BCD format, as MAJ.MIN with a range from 1.0 to 9.9, with the initial silicon revision reporting revision 1.0 (10h).

Table 42. PROD_REV register (address 12h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	PROD_REV_MAJ[3:0]				PROD_REV_MIN[3:0]			
Reset	0	0	0	1	0	0	1	1
Access	R	R	R	R	R	R	R	R

Table 43. PROD_REV register (address 12h) bit description

Field	Description
7 to 4 PROD_REV_MAJ[3:0]	Product revision info, major product revision value with range 1 to 9 in BCD format.
3 to 0 PROD_REV_MIN[3:0]	Product revision info, minor product revision value with range 0 to 9 in BCD format.

15.9 WHO_AM_I register (address 13h)

This register contains the NXP unique sensor product identifier and is factory programmed to 87h for FXLS8967AF.

Table 44. WHO_AM_I register (address 13h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	WHO_AM_I[7:0]							
Reset	1	0	0	0	0	1	1	1
Access	R	R	R	R	R	R	R	R

15.10 SYS_MODE register (address 14h)

The **SYS_MODE** register indicates the current device operating mode. Applications using the Auto-WAKE/SLEEP mechanism should use this register to synchronize their application with FXLS8967AF operating mode transitions. This register also indicates the status of the buffer gate error flag and the buffer gate count.

Table 45. SYS_MODE register (address 14h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	BUF_ GATE_ ERR	BUF_GATE_CNT[4:0]					SYS_MODE[1:0]	
Reset (BT_MODE = GND)	0	—	—	—	—	—	0	0
Reset (BT_MODE = V_{DD})	0	—	—	—	—	—	0	1
Access	R	R	R	R	R	R	R	R

Table 46. SYS_MODE register (address 14h) bit description

Field	Description
7 BUF_GATE_ERR	Buffer gate error flag: 0: A buffer gate error has not been detected 1: A buffer gate error was detected. If **BUF CONFIG1[**BUF _GATE**]** = 1 and the output buffer is not emptied before the arrival of the next XYZ acceleration sample, the BUF _GATE_ERR flag is asserted. The BUF GATE_ERR flag remains asserted as long as the output buffer remains un-emptied. The BUF GATE_ERR flag may be cleared in one of the following ways: 1. Reading out the entire contents of the output buffer such that **BUF _STATUS[**BUF_CNT[5:0]**]** = 0. 2. Flushing (clearing) the output buffer contents by setting **BUF_CONFIG2[**BUF _FLUSH**]** = 1. 3. Disabling the output buffer by setting **BUF _CONFIG1[**BUF MODE[1:0]**]** = 00b, which clears BUF_CNT. 4. Transitioning FXLS8967AF from Standby to Active mode.

Table 46. SYS_MODE register (address 14h) bit description*...continued*

Field	Description
6 to 2 BUF_GATE_CNT[4:0]	The BUF_GATE_CNT field contains the number of OOR periods that have elapsed since the BUF _GATE_ERR flag was asserted. This buf_gate_cnt field is reset to 0 after any of the following actions: 1. The host reads out the entire contents of the output buffer such that **BUF STATUS[**BUF_CNT[5:0]**]** = 0. 2. The host flushes (clears) the output buffer by setting **BUF _CONFIG2[**BUF _FLUSH**]** = 1. 3. Disable the output buffer by setting **BUF CONFIG1[**BUF _MODE[1:0]**]** = 00b, which also clears the buffer contents. 4. Transitioning FXLS8967AF from Standby to Active mode. which also clears the buffer contents.
1 to 0 SYS_MODE[1:0]	The current system operating mode 00b: Standby mode (default mode after a POR or soft reset event when BT_MODE = GND) 01b: WAKE mode (default mode after a POR or soft reset event when BT_MODE = V_{DD} and MOT_DET = 1) 10b: SLEEP mode 11b: EXT_TRIG mode (this mode is unavailable when BT_MODE = V_{DD}) ***Notes:*** • *When external trigger mode is enabled (with **SENS_CONFIG4[**INT2_FUNC**]** = 1), while the device is waiting for a trigger event to occur, SYS_MODE[1:0] is set to 11b. When the trigger is received, SYS_MODE[1:0] is set to 01b while the measurement is being made, and then change back to 11b and remain there until the next trigger signal is received.* • *When **INT_EN[**WAKE_OUT_EN**]** = 1, and SYS_MODE[1:0] = 01b (WAKE), the device outputs either a logic '1' or '0' on either the INT1 or INT2 pins, depending on the settings made in **INT_PIN_SEL[**WAKE_OUT_INT2**]** and **SENS_CONFIG4[**INT_POL**]**.* • *When entering the WAKE, SLEEP, or EXT_TRIG modes, the internal debounce counters for the ORIENT, SDCD_WT, and SDCD_OT event functions are automatically reset.*

15.11 SENS_CONFIG1 register (address 15h)

Table 47. SENS_CONFIG1 register (address 15h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	RST	ST_AXIS_SEL[1:0]		ST_POL	SPI_M	FSR[1:0]		ACTIVE
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	0	0	0	0	0	0	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 48. SENS_CONFIG1 register (address 15h) bit description

Field	Description
7 RST	The RST bit may be used to initiate a software reset. The reset mechanism can be triggered in Standby, Active (WAKE or SLEEP), and EXT_TRIG operating modes. When the RST bit is set, the boot mechanism resets all functional blocks and loads the internal registers with their default values (The **INT_POL, INT_PP_OD**, and **BOOT_DIS** bits are not reset and maintains their current values as long as power is not removed from the V_{DD} pin and Hibernate mode is not enabled). The host application should allow T_{BOOT1} or T_{BOOT2} ms between issuing a reset command and attempting communications with FXLS8967AF over the I^2C/SPI interfaces. Alternatively, the host can wait for the active edge on the $T_{BOOT1/2}$ pulse event signaled on the configured INTx pin. 0: No device reset pending 1: Write '1' to trigger the soft reset sequence ***Notes:*** • *The I^2C and SPI interface blocks are also reset to avoid corrupted data transactions.* • *The reset sequence does not start until the host I^2C controller issues the SP (stop) condition, or the SPI primary releases the SPI_CS_B pin.* • *The host always reads back this bit as '0'.* • *There is a delay of 300 µs to 500 µs between setting the RST bit and the commencement of the reset sequence.*
6 to 5 ST_AXIS_SEL[1:0]	Self-test axis selection This bit field selects the transducer axis to test using the Self-Test function. The ST_POL bit allows either positive or negative self-test displacements to be applied. The host system may use the self-test function to verify the functionality of both the transducer and signal measurement chain without the need to apply an external acceleration stimulus. ***Notes:*** • *The data output from the two axes that are not selected by **ST_AXIS_SEL** during the self-test sequence are not meaningful and should be ignored.* • *NXP recommends minimizing the communication traffic on the device serial interface during the measurement phase in order to reduce the susceptibility of the self-test response signal to induced noise. NXP strongly recommends operating the self-test in interrupt mode.* 00b: (default): Self-test function is disabled 01b: Self-test function is enabled for X-axis 10b: Self-test function is enabled for Y-axis 11b: Self-test function is enabled for Z-axis
4 ST_POL	Self-test displacement polarity 0 (default): Proof mass displacement for the selected axis is in the positive direction. 1: Proof mass displacement for the selected axis is in the negative direction.
3 SPI_M	SPI interface mode selection; selects between 3- and 4-wire operating modes for the SPI interface: 0 (default): 4-wire interface mode is selected 1: 3-wire interface mode is selected ***Notes:*** • *The state of this bit is only relevant when the SPI interface mode is selected (INTF_SEL = V_{DD}).* • *When INTF_SEL = V_{DD} and SPI_M = 1, the SDA/SPI_MOSI pin becomes the bidirectional SPI_DATA pin; the SA0/MISO pin is unused and placed in a high-impedance state.* • *4-wire mode is selected by default after a POR/BOR event or when exiting Hibernate mode.* • *If INTF_SEL = V_{DD} and the SPI_MOSI and SPI_MISO lines are directly connected together on the PCB, 3-wire SPI mode is enabled regardless of the setting of this bit*

Table 48. SENS_CONFIG1 register (address 15h) bit description*...continued*

Field	Description
2 to 1 FSR[1:0]	Full-scale measurement range (FSR) selection 00b: ±2 *g*; 0.98 m*g*/LSB (1024 LSB/*g*) nominal sensitivity 01b (default): ±4 *g*; 1.95 m*g*/LSB (512 LSB/*g*) nominal sensitivity 10b: ±8 *g*; 3.91 m*g*/LSB (256 LSB/*g*) nominal sensitivity 11b: ±16 *g*; 7.81 m*g*/LSB (128 LSB/*g*) nominal sensitivity
0 ACTIVE	Standby/Active mode selection This bit selects between Standby mode and Active mode. ***Note:*** • *When INT2_FUNC = 1, the Active bit becomes read only via the I^2C or SPI interface as the INT2 pin logic state directly controls the device operating mode. The INT2_FUNC may only be enabled (set to 1) when ACTIVE = 0. Similarly, the ACTIVE bit may only be set if INT2_FUNC = 0.* 0: FXLS8967AF is placed in Standby mode and draws the minimum amount of current on the V_{DD} pin ($I_{DD-STBY}$). Standby mode is the default mode after a POR or soft reset event. 1: FXLS8967AF is placed in Active mode and draws an I_{DD} corresponding to the selected ODR in HPM, the selected ODR in LPM, or the user-selected decimation and idle time settings in FPM.

15.12 SENS_CONFIG2 register (address 16h)

Table 49. SENS_CONFIG2 register (address 16h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	WAKE_PM[1:0]		SLEEP_PM[1:0]		LE_BE	—	AINC_ TEMP	F_READ
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 50. SENS_CONFIG2 register (address 16h) bit description

Field	Description
7 to 6 WAKE_PM[1:0]	WAKE power mode selection 00b: Low-power mode is selected; **SENS_CONFIG3[**7:4**]** bits are interpreted as WAKE_ODR[3:0] and sets the ODR and decimation factor as per Table 52. 01b: High performance mode is selected; **SENS_CONFIG3[**7:4**]** bits are interpreted as WAKE_ODR[3:0] and set the ODR and decimation factor as per Table 53. 1xb: Flexible performance mode is selected; **SENS_CONFIG3[**7:4**]** bits are interpreted as WAKE_DEC[3:0], which sets the measurement decimation factor. The effective ODR (and measurement current) is determined by the combination of the decimation factor and the 12-bit measurement idle time programmed in the **WAKE_IDLE_MSB** and **WAKE_IDLE_LSB** registers. See Table 54 for the selectable decimation factors. ***Note:*** *In motion detection mode with BT_MODE=V_{DD}, use of HPM or FPM mode is not advised. Only the default LPM mode should be used.*

Table 50. SENS_CONFIG2 register (address 16h) bit description*...continued*

Field	Description
5 to 4 SLEEP_PM[1:0]	SLEEP power mode selection 00b: Low-power mode is selected; **SENS_CONFIG3[**3:0**]** bits are interpreted as SLEEP_ODR[3:0] and sets the ODR and decimation factor as per Table 52. 01b: High performance mode is selected; **SENS_CONFIG3[**3:0**]** bits are interpreted as SLEEP_ODR[3:0] and set the ODR and decimation factor as per Table 53. 1xb: Flexible performance mode is selected; **SENS_CONFIG3[**3:0**]** bits are interpreted as SLEEP_DEC[3:0], which sets the measurement decimation factor. The effective ODR (and measurement current) is determined by the combination of the decimation factor and the 12-bit measurement idle time programmed in the **SLEEP_IDLE_MSB** and **SLEEP_IDLE_LSB** registers. See Table 54 for the selectable decimation factors. ***Note:*** *In motion detection mode with BT_MODE=V_{DD}, use of HPM or FPM mode is not advised. Only the default LPM mode should be used.*
3 LE_BE	Little/Big-endian output mode selection 0: Little-endian output mode is selected; the output data LSBs are stored at the lower logical address and the MSBs (nibbles) are right-justified. 1: Big-endian output mode is selected; the output data MSBs are stored at the lower logical address and the LSBs (nibbles) are left justified. ***Note:*** *The output data format selection applies only to the data read from the **OUT_X/Y/Z**, **VECM**, and **BUF_X/Y/Z** registers. All other multi-byte fields within the device are fixed in little-endian right justified format.*
1 AINC_TEMP	Temperature output data auto-increment control 0 (default): **TEMP_OUT** register content is not included in auto-increment address range. 1: **TEMP_OUT** register content is included in auto-increment address range.
0 F_READ	Fast-read mode selection When this bit is set, the output data format is limited to the most significant byte of the 12-bit sample. The MSB data is always stored in the lower address, regardless of the setting made in **SENS_CONFIG1[**LE_BE**]**. The auto-increment address pointer automatically skips over the higher address for each axis' sample when performing a burst read operation of the current output data or buffered data when the F_READ bit is set. 0: Normal read mode 1: Fast-read mode

15.13 SENS_CONFIG3 register (address 17h)

The SENS_CONFIG3 register is used to set the WAKE and SLEEP ODRs when operating in low-power mode or High Performance Mode, and the decimation factor for WAKE and SLEEP modes in Flexible Power Mode.

Notes:

- *In motion detection mode with BT_MODE=V_{DD}, use of HPM or FPM mode is not advised. Only the default LPM mode should be used.*
- *When BT_MODE=VDD, maximum recommended ODR is 100 Hz. When the data ready interrupt is enabled, the interrupt line (INT1) will pulse low for TPULSE-MOT seconds (**5 ms typ**) for every ODR period. Therefore, for higher ODRs, the host does not observe DRDY interrupt pulse at every ODR period.*

Table 51. SENS_CONFIG3 register (address 17h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	WAKE_ODR[3:0] / WAKE_DEC[3:0]				SLEEP_ODR[3:0] / SLEEP_DEC[3:0]			
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	1	1	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

In HPM and LPM modes, a decimation factor is implicit, as specified in Table 52 and Table 53, respectively.

In FPM, the decimation factor for WAKE and SLEEP modes is specified via the same bit-fields (see Table 54 for the available settings), and along with the WAKE and SLEEP idle time parameter determines the effective ODR.

For example, if **SENS_CONFIG2[**WAKE_PM**]** = 10b, selecting FPM in the WAKE operating mode, the SENS_CONFIG3 upper nibble is interpreted as the decimation factor for WAKE mode (WAKE_DEC[3:0]) per Table 54. If a value of 0110b is chosen, for example, a decimation factor of 64 is selected. If WAKE_IDLE[11:0] is set to 256 (decimal), the effective ODR would be 1 / ((256+1) * (312.5 µs) * 64) = 0.195 Hz.

The effective ODR is determined in a similar manner for the SLEEP operating mode using the SLEEP_DEC[3:0] and the SLEEP_IDLE[11:0] values.

When operating in HPM or LPM with ODR = 3200 Hz, or in FPM with IDLE_TIME = 0, the first data sample is produced after a time delay greater than 1 ODR period using Equation 1.

$$T_{DELAY}(s) = 528.5\ \mu s + 0.9984\ \times (DEC - 1)\ \times \left(\frac{1}{(ODR \times DEC)}\right) \quad (1)$$

Note: *The IDLE_TIME refers to either WAKE_IDLE[11:0] or SLEEP_IDLE[11:0], depending on current operating mode.*

After this initial delay, all subsequent data samples are made available at the ODR rate. For all other operating modes and settings the first sample is produced within 1 ODR period.

Notes:

- *When the device transitions from WAKE to SLEEP or from SLEEP to WAKE modes there is a 500 µs (nominal) delay between the last acquisition at the WAKE/SLEEP mode ODR and the first acquisition at the SLEEP/WAKE mode ODR.*
- *The ODR may only be changed in Standby mode, with **SENS_CONFIG1[**ACTIVE**]** = 0 and **SENS_CONFIG4[**INT2_FUNC**]** = 0.*

Table 52. WAKE and SLEEP low-power mode ODR and decimation settings

ODR[3]	ODR[2]	ODR[1]	ODR[0]	ODR Selection (Hz)	Decimation selection (samples)	Noise RMS (mg)[1][2]	I_{DD} (µA)
0	0	0	0	3200	1	12.39	150
0	0	0	1	1600	1	11.77	75
0	0	1	0	800	1	11.19	38

Table 52. WAKE and SLEEP low-power mode ODR and decimation settings *...continued*

ODR[3]	ODR[2]	ODR[1]	ODR[0]	ODR Selection (Hz)	Decimation selection (samples)	Noise RMS (mg)[1][2]	I_{DD} (µA)
0	0	1	1	400	1	10.91	20
0	1	0	0	200	1	10.71	11
0	1	0	1	100	1	10.63	5.3
0	1	1	0	50	1	10.71	3.1
0	1	1	1	25	1	10.66	1.8
1	0	0	0	12.5	1	10.65	1.4
1	0	0	1	6.25	1	10.69	1.0
1	0	1	0	3.125	1	10.77	0.80
1	0	1	1	1.563	1	10.63	0.70
1	1	0	0	0.781	1	10.57	0.65
1	1	0	1	0.781	1	10.57	0.65
1	1	1	0	0.781	1	10.57	0.65
1	1	1	1	0.781	1	10.57	0.65

[1] Values are for ±2 *g* FSR only.
[2] Based on post board mount characterization data. Tested on a mechanically isolated granite table to provide isolation from environmental vibration.

Table 53. WAKE and SLEEP High Performance mode ODR and decimation settings

ODR[3]	ODR[2]	ODR[1]	ODR[0]	ODR selection (Hz)	Decimation selection (samples)	Noise RMS (mg)[1][2]	I_{DD} (µA)
0	0	0	0	3200	1	12.51	150
0	0	0	1	1600	2	8.57	150
0	0	1	0	800	4	5.79	150
0	0	1	1	400	8	4.00	150
0	1	0	0	200	16	2.80	150
0	1	0	1	100	32	1.98	150
0	1	1	0	50	64	1.40	150
0	1	1	1	25	128	1.01	150
1	0	0	0	12.5	256	0.74	150
1	0	0	1	6.25	512	0.56	150
1	0	1	0	3.125	1024	0.49	150
1	0	1	1	1.563	2048	0.40	150
1	1	0	0	0.781	4096	0.29	150
1	1	0	1	0.781	4096	0.29	150
1	1	1	0	0.781	4096	0.29	150

Table 53. WAKE and SLEEP High Performance mode ODR and decimation settings*...continued*

ODR[3]	ODR[2]	ODR[1]	ODR[0]	ODR selection (Hz)	Decimation selection (samples)	Noise RMS (mg)[1][2]	I_{DD} (µA)
1	1	1	1	0.781	4096	0.29	150

[1] Values are for ±2 *g* FSR only.
[2] Based on post board mount characterization data. Tested on a mechanically isolated granite table to provide isolation from environmental vibration.

Table 54. WAKE and SLEEP decimation settings in Flexible Power mode

DEC[3]	DEC[2]	DEC[1]	DEC[0]	Decimation selection (samples)	Measurement time (ms)
0	0	0	0	1	0.3125
0	0	0	1	2	0.625
0	0	1	0	4	1.25
0	0	1	1	8	2.5
0	1	0	0	16	5
0	1	0	1	32	10
0	1	1	0	64	20
0	1	1	1	128	40
1	0	0	0	256	80
1	0	0	1	512	160
1	0	1	0	1024	320
1	0	1	1	2048	640
1	1	0	0	4096	1280
1	1	0	1	4096	1280
1	1	1	0	4096	1280
1	1	1	1	4096	1280

15.14 SENS_CONFIG4 register (address 18h)

Table 55. SENS_CONFIG4 register (address 18h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	EXT_ TRIG_M	WAKE_ SDCD_WT	WAKE_ SDCD_OT	WAKE_ ORIENT	DRDY_PUL	INT2_FUNC	INT_ PP_OD	INT_POL
Reset	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 56. SENS_CONFIG4 register (address 18h) bit description

Field	Description
7 EXT_TRIG_M	External trigger function acquisition mode. 0 (default): Each positive going trigger edge causes a single ADC acquisition to be made. When the number of acquisitions specified by the current operating mode decimation setting have been triggered, the final decimated output is stored in the **OUT_X/Y/Z** registers or the buffer depending on the setting made in **BUF_CONFIG1[**BUF_MODE[1:0]**]**. . 1: Each positive going trigger edge causes multiple ADC acquisitions. The number of acquisitions are specified by the current operating mode decimation setting[1]. Once the specified number of acquisitions have been made, the final decimated output is stored in the **OUT_X/Y/Z** registers or the buffer depending on the setting made in **BUF_CONFIG1[**BUF_MODE[1:0]**]**. ***Notes:*** • *The EXT_TRIG_M setting only applies when INT2_FUNC = 1.* • *The SRC_DRDY event flag is asserted after the specified number of measurements have completed and the final decimated output result is available. Note that the SRC_DRDY flag is only asserted when **BUF_CONFIG1[**BUF_MODE[1:0]**]** = 00b* • *In LPM, this bit has no effect as the decimation factor is fixed at 1.*
6 WAKE_SDCD_WT	SDCD within thresholds event Auto-WAKE/SLEEP transition source enable 0 (default): SDCD within thresholds event is not used to prevent entry into/trigger an exit from SLEEP mode. 1: SDCD within thresholds event is used to prevent entry into/trigger an exit from SLEEP mode.
5 WAKE_SDCD_OT	SDCD outside of thresholds event Auto-WAKE/SLEEP transition source enable 0 (default): SDCD outside of thresholds event is not used to prevent entry into/trigger an exit from SLEEP mode. 1: SDCD outside of thresholds event is used to prevent entry into/trigger an exit from SLEEP mode.
4 WAKE_ORIENT	Orientation change event Auto-WAKE/SLEEP transition source enable 0 (default): Orientation change condition is not used as an event to prevent entry into /trigger an exit from SLEEP mode. 1: Orientation change condition is used as an event to prevent entry into/trigger an exit from SLEEP mode.
3 DRDY_PUL	Pulse generation option for DRDY event 0 (default): A SRC_DRDY event is output on the INTx pin as an active high or active low signal depending on the polarity setting made in INT_POL. The INTx pin remains asserted until the host reads any of the OUT_X/Y/Z registers. 1: A 32 µs (nominal) duration pulse is output on the configured INTx pin once per ODR cycle. The output pulse is either positive or negative, depending on the INT_POL setting. ***Notes:*** • *The pulsed output signal is OR'd with all of the other interrupt events assigned to the INTx pin.* • *In Motion Detection mode (BT_MODE = V_{DD}), the state of this bit is ignored and has no effect on device operation.*

Table 56. SENS_CONFIG4 register (address 18h) bit description*...continued*

Field	Description
2 INT2_FUNC	INT2 output / EXT_TRIG input pin selection 0 (default): INT2/EXT_TRIG pin is configured for the INT2 output function. The logic polarity and output driver type are specified in the **INT_POL** and **INT_PP_OD** registers. Interrupt signals are selectively routed to this output pin using the **INT_PIN_SEL** register. 1: INT2/EXT_TRIG pin is configured as the EXT_TRIG input function. A positive edge (low-to-high) transition on the EXT_TRIG pin is used to trigger either a single measurement of the acceleration and temperature data using the current decimation settings when EXT_TRIG_M = 1 or a single acquisition of the current acceleration and temperature data when EXT_TRIG_M = 0. This function is useful for realizing low frequency or asynchronous ODRs initiated by the host system, for example, by using an MCU timer output pin. When this function is enabled, it is reflected in the **SYS_MODE** register. ***Notes:*** • *When the EXT_TRIG function is enabled, any bits set to '1' in the **INT_PIN_SEL** register (mapping an event flag to the INT2 output pin) are ignored as the pin becomes a dedicated high-impedance input pin for the external trigger function.* • *The INT2_FUNC bit setting is ignored when BT_MODE = V_{DD} as the external trigger function is not available in this mode.*
1 INT_PP_OD	INT1 and INT2 pins output driver selection 0 (default): INTx output pin driver is push-pull type. 1: INTx output pin driver is open-drain/open-source type. An external pull-up/pull-down resistor is required. ***Notes:*** • *If a user operation sets INT_PP_OD before issuing a soft reset command, the setting is maintained through the reset sequence (only lost when V_{DD} supply is removed or Hibernate mode is enabled).* • *The INT_PP_OD bit setting is ignored when BT_MODE = V_{DD} as the INT1/MOT_DET and INT2/BOOT_OUT output driver type is fixed to open-drain.*
0 INT_POL	Interrupt logic polarity on INT1 and INT2 pins Selects the polarity of the interrupt output signal on the INT1 and INT2 pins. 0: Active low: interrupt events are signaled with a logical '0' level. If DRDY_PUL=1, a SRC_DRDY event pulse is negative going. The inactive state of the INTx pins is logic '1' (V_{DD}). 1 (default): Active high: interrupt events are signaled with a logical '1' level. If DRDY_PUL=1, a SRC_DRDY event pulse is positive going. The inactive state of the INTx pins is logic '0' (GND). ***Notes:*** • *If a user operation sets INT_POL before issuing a soft reset command, the setting is maintained through the reset sequence (only lost if V_{DD} supply is removed or Hibernate mode is enabled).* • *The INT_POL bit setting is ignored when BT_MODE = V_{DD} as the INT1/MOT_DET and INT2/BOOT_OUT interrupt logic polarity is fixed at active low (external pull-up resistors are required).*

[1] In order to acquire all the measurements specified by the decimation setting, only one trigger event is needed.

Table 57. INTx pin behavior as a function of INT_PP_OD and INT_POL bit settings (valid only when BT_MODE = V_{DD})

INTx pin configuration	INT_PP_OD	INT_POL	INTx pin asserted value	INTx pin deasserted value
CMOS output	0	0	0	1
CMOS output	0	1	1	0
External pull-up resistor added (open-drain)	1	0	0	High-Z[1]

Table 57. INTx pin behavior as a function of INT_PP_OD and INT_POL bit settings (valid only when BT_MODE = V_{DD})*...continued*

INTx pin configuration	INT_PP_OD	INT_POL	INTx pin asserted value	INTx pin deasserted value
External pull-down resistor added (open source)	1	1	1	High-Z[1]

[1] High-Z means high impedance condition, with the state of the INTx pin defined by the external pull-up or pull-down resistor.

Table 58. INTx pin behavior as a function of INT_PP_OD and INT_POL bit settings (valid only when BT_MODE = V_{DD})

INTx pin configuration	INT_PP_OD	INT_POL	INTx pin asserted value	INTx pin deasserted value
External pull-up resistor added (open-drain)	X	X	0	1

15.15 SENS_CONFIG5 register (address 19h)

Table 59. SENS_CONFIG5 register (address 19h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	VECM_EN	X_DIS	Y_DIS	Z_DIS	HIBERNATE_EN
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 60. SENS_CONFIG5 register (address 19h) bit description

Field	Description
4 VECM_EN	Vector Magnitude calculation enable: 0 (default): 12-bit vector magnitude result is not calculated on every ODR cycle. The VECM_LSB and VECM_MSB registers are not included in auto-increment address range. 1: 12-bit vector magnitude result *is* calculated on every ODR cycle. The VECM_LSB and VECM_MSB registers are included in auto-increment address range. ***Note:*** *The vector magnitude result may also be used as an input to the SDCD function when* ***SDCD_CONFIG2[****MODE****]*** *= 1.*
3 X_DIS	X-axis auto-increment disable: 0 (default): X-axis measurement is included in the auto-increment address range for both buffered and non-buffered modes (default). 1: X-axis measurement is excluded from the auto-increment address range.
2 Y_DIS	Y-axis auto-increment disable: 0 (default): Y-axis measurement is included in the auto-increment address range for both buffered and non-buffered modes (default). 1: Y-axis measurement is excluded from the auto-increment address range.

Table 60. SENS_CONFIG5 register (address 19h) bit description*...continued*

Field	Description
1 Z_DIS	Z-axis auto-increment disable: 0 (default): Z-axis measurement is included in the auto-increment address range for both buffered and non-buffered modes (default). 1: Z-axis measurement is excluded from the auto-increment address range.
0 HIBERNATE_EN	Hibernate mode enable: 0: Hibernate mode not enabled; device is operating per the mode selected in WAKE_PM/SLEEP_PM[1:0] 1: Commands device to enter Hibernate mode; all RAM register contents are lost. ***Notes:*** • *When BT_MODE = GND:* *When Hibernate Mode is selected, FXLS8967AF is completely shut down (similar to removing the V_{DD} supply), with all register contents lost. To exit Hibernate Mode, a positive or negative going edge must be applied to the SPI_CS_B/WAKE_UP pin (logic level must toggle from the state applied at the time this bit was set). The host must then wait T_{BOOT1} ms for the part to re-enter Standby mode before attempting communications over the I^2C or SPI interfaces.* • *When BT_MODE = V_{DD}:* *Hibernate mode is automatically entered/exited based on the level input to the MOT_DET pin. The part directly enters Active mode with the preconfigured motion detection settings when MOT_DET is pulled high. The host must wait T_{BOOT2} ms for the boot process to complete and the motion detection process to begin. When MOT_DET is brought low, the part automatically enters Hibernate mode to conserve power.*

15.16 WAKE_IDLE_LSB register (address 1Ah)

This register, along with WAKE_IDLE_MSB, sets the unsigned 12-bit WAKE mode idle time (off time).

Note: *The contents of this register are only meaningful when* ***SENS_CONFIG2[****WAKE_PM[1:0]****]*** *= 1xb.*

The counter period is nominally 312.5 µs/LSB, providing a range of 312.5 µs to 1.28 seconds. The idle time + measurement time (set by the WAKE mode decimation factor) forms the measurement period (ODR^{-1}) as described in the Section 15.13 register description.

Table 61. WAKE_IDLE_LSB register (address 1Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	WAKE_IDLE[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15.17 WAKE_IDLE_MSB register (address 1Bh)

Flexible Power Mode WAKE idle time MSB. The contents of this register are only meaningful when **SENS_CONFIG2[**WAKE_PM[1:0]**]** = 1xb.

Table 62. WAKE_IDLE_MSB register (address 1Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	0	0	0	0	WAKE_IDLE[11:8]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15.18 SLEEP_IDLE_LSB register (address 1Ch)

Flexible Power Mode SLEEP idle time LSB. The contents of this register are only meaningful when **SENS_CONFIG2[**SLEEP_PM[1:0]**]** = 1xb. This register, along with SLEEP_IDLE_MSB, sets the unsigned 12-bit SLEEP mode idle-time (off-time). The counter time period is 312.5 µs/LSB, providing a range of 312.5 µs to 1.28 seconds. The idle time + measurement time (set by the SLEEP mode decimation factor) forms the measurement period (ODR^{-1}).

Table 63. SLEEP_IDLE_LSB register (address 1Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	SLEEP_IDLE[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15.19 SLEEP_IDLE_MSB register (address 1Dh)

Flexible Power Mode SLEEP idle time MSB (nibble). The contents of this register are useful only when **SENS_CONFIG2[**SLEEP_PM[1:0]**]** = 1xb.

Table 64. SLEEP_IDLE_MSB register (address 1Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	0	0	0	0	SLEEP_IDLE_TIME[11:8]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15.20 ASLP_COUNT_LSB, ASLP_COUNT_MSB registers (addresses 1Eh to 1Fh)

The **ASLP_COUNT** value sets the minimum number of ODR periods needed to transition from WAKE to SLEEP mode when no event activity is detected. See Section 15.14 for events that may be monitored for inactivity in order to trigger the transition to SLEEP mode when the internal counter reaches the **ASLP_COUNT** value.

The sleep counter period corresponds to the selected WAKE mode ODR period when operating in LPM and HPM, and to the effective ODR set by the WAKE decimation (measurement time) and WAKE idle time (off-time) settings when the device operates in FPM. The auto-WAKE/SLEEP feature is only enabled when the value written to ASLP_CNT is > 0.

SENS_CONFIG2[WAKE_PM**]** sets the WAKE power mode;
SENS_CONFIG3[WAKE_ODR**]** sets the ODR. When operating in Flexible Performance Mode, **SENS_CONFIG3[**WAKE_DEC**]** and **WAKE_IDLE[**11:0**]** values set the effective ODR.

SENS_CONFIG2[SLEEP_PM**]** sets the SLEEP power mode; **SENS_CONFIG3[**SLEEP_ODR**]** sets the ODR. When operating in Flexible Performance Mode, **SENS_CONFIG3[**SLEEP_DEC**]** and **SLEEP_IDLE[**11:0**]** values set the effective ODR.

The functions used to detect inactivity and enter SLEEP mode upon expiry of the **ASLP_COUNT** timer (see Table 69) are selected in **SENS_CONFIG4** and **BUF_CONFIG2**. The same functions used to enter SLEEP are also used to exit this mode when activity is detected except for the SRC_BUF event flag, which can only be used to prevent/delay a transition from WAKE to SLEEP if the host system is reading data from the buffer (and clearing SRC_BUF). A transition from SLEEP to WAKE mode occurs as soon as one of the enabled detection events becomes active. See Table 70 for the corresponding Interrupt event sources.

Table 65. ASLP_COUNT_LSB register (address 1Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	ASLP_COUNT[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 66. ASLP_COUNT_LSB register (address 1Eh) bit description

Field	Description
7 to 0 ASLP_COUNT [7:0]	LSB of the 12-bit unsigned count value used for inactivity detection. The selected WAKE mode ODR determines the counter period.

Table 67. ASLP_COUNT_MSB register (address 1Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	ASLP_COUNT[11:8]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 68. ASLP_COUNT_MSB register (address 1Fh) bit description

Field	Description
3 to 0 ASLP_COUNT [11:8]	MSB (nibble) of the 12-bit unsigned count value used for inactivity detection. The selected WAKE mode ODR determines the counter period.

Table 69. ASLP_COUNT timer period

WAKE mode ODR (Hz)	WAKE mode ODR Period (ms)	ASLP_COUNT Period (ms)	Max Inactivity Times
3200	0.3125	0.3125	1.28
1600	0.625	0.625	2.56
800	1.25	1.25	5.12

Table 69. ASLP_COUNT timer period*...continued*

WAKE mode ODR (Hz)	WAKE mode ODR Period (ms)	ASLP_COUNT Period (ms)	Max Inactivity Times
400	2.5	2.5	10.24
200	5	5	20.48
100	10	10	40.96
50	20	20	81.92
25	40	40	163.84
12.5	80	80	327.68
6.25	160	160	655.36
3.125	320	320	1310.72
1.563	640	640	2621.44
0.781	1280	1280	5242.54

Table 70. Auto-WAKE/SLEEP Interrupt Event Sources

Interrupt Event Source	Event flag can clear auto-sleep timer?	Event flag can transition the device from SLEEP to WAKE mode?
SRC_DRDY	No	No
SRC_OVF	No	No
SRC_BUF	Yes[1]	No
SRC_SDCD_OT	Yes	Yes
SRC_SDCD_WT	Yes	Yes
SRC_ORIENT	Yes	Yes
SRC_ASLP	No[2]	No[2]
SRC_BOOT	No	No

[1] When BUF_CONFIG2[WAKE_SRC_BUF] = 1, clearing the SRC_BUF event flag resets the auto-sleep timer and prevent FXLS8967AF from entering SLEEP mode. When BUF_CONFIG2[WAKE_SRC_BUF] = 0 (default), FXLS8967AF enters SLEEP mode regardless of the state of the BUF_WMRK or BUF_OVF event flags.

[2] If the BUF_GATE bit is set to logic '1', it prevents the output buffer from accepting new data after a WAKE-to-SLEEP or SLEEP-to-WAKE operating mode transition until the host first empties the buffer contents. The BUF_GATE bit is useful for preventing acceleration data from different WAKE and SLEEP mode ODRs from being mixed within the buffer.

15.21 INT_EN register (address 20h)

This register is used to enable and disable the various interrupt event generators embedded within the device.

Note:

- *When BT_MODE = V_{DD}, the INT1/MOT_DET pin signals any mapped (and enabled) interrupts with a $T_{PULSE-MOT}$ ms active low pulse (open-drain output with external pull-up).*
- *Any enabled interrupt is signaled with a $T_{PULSE-MOT}$ ms pulse at the ODR rate until the respective interrupt source flag is cleared.*

- *The INT2/BOOT_OUT pin only signals the boot process complete interrupt, signaled by a $T_{PULSE-BOOT2}$ ms active low pulse (open-drain with external pull-up). Any other interrupt sources mapped to the INT2/BOOT_OUT pin are ignored.*

Table 71. INT_EN register (address 20h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	DRDY_EN	BUF_EN	SDCD_ OT_EN	SDCD_ WT_EN	ORIENT_ EN	ASLP_EN	BOOT_ DIS	WAKE_ OUT_EN
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 72. INT_EN register (address 20h) bit description

Field	Description
7 DRDY_EN	Data-ready interrupt output enable 0 (default): Interrupt is disabled. 1: Interrupt is enabled and signaled on either the INT1 or INT2 output pins as configured by the setting made in INT_PIN_SEL. ***Note:*** *When BT_MODE = GND, SRC_DRDY bit and the signaled interrupt are cleared whenever one or more of the VECM, and OUT_X/Y/Z registers are read. When BT_MODE = V_{DD}, SRC_DRDY bit is cleared whenever one or more of the VECM, and OUT_X/Y/Z registers are read. However the data ready interrupt is signaled for TPULSE-MOT s (5 ms typ) and it clears itself automatically. The current data ready interrupt pulse is terminated when the device transitions into STANDBY mode before its completion and therefore may not span for entire TPULSE-MOTs.*
6 BUF_EN	Output data buffer interrupt output enable 0 Interrupt is not routed to the INTx output pins (default) 1: Interrupt is routed to either the INT1 or INT2 output pins as configured by the setting made in **INT_ PIN_SEL**.
5 SDCD_OT_EN	SDCD outside of thresholds interrupt output enable 0 (default): Interrupt is disabled. 1: Interrupt is routed to either the INT1 or INT2 output pin as configured by the setting made in INT_ PIN_SEL.
4 SDCD_WT_EN	SDCD within thresholds interrupt output enable 0 (default): Interrupt is disabled. 1: Interrupt is routed to either the INT1 or INT2 output pins as configured by the setting made in INT_ PIN_SEL.
3 ORIENT_EN	Orientation interrupt output enable 0 (default): Interrupt is disabled. 1: Interrupt is enabled and signaled on either the INT1 or INT2 output pins as determined by the setting made in INT_PIN_SEL.
2 ASLP_EN	Auto-WAKE/SLEEP interrupt output enable 0 (default): Interrupt is disabled. 1: Interrupt is enabled and signaled on either the INT1 or INT2 output pins as determined by the setting made in INT_PIN_SEL.

Table 72. INT_EN register (address 20h) bit description*...continued*

Field	Description
1 BOOT_DIS	Boot interrupt output disable 0 (default): Boot interrupt is enabled and routed to either the INT1 or INT2 output pin as determined by the setting made in **INT_PIN_SEL**. This interrupt is pulsed, with the polarity of the pulse determined by the setting made in **SENS_CONFIG4[**INT_POL**]**. 1: Interrupt is disabled and not routed to the INTx output pins. **When BT_MODE = GND:** The SRC_BOOT interrupt is signaled on the INTx pin selected in **INT_PIN_SEL** and pulsed for a duration of $T_{PULSE-BOOT1}$ µs when the BOOT process completes. **When BT_MODE = V_{DD}:** This bit is ignored and the SRC_BOOT interrupt is internally enabled and mapped to the INT2/BOOT_OUT pin (fixed settings). The INT2/BOOT_OUT pin is pulsed low for a duration of $T_{PULSE-BOOT2}$ ms during the BOOT sequence. ***Note:*** *The BOOT_DIS bit holds the user programmed value until the V_{DD} supply is removed or Hibernate mode is entered; this setting is, however, maintained across a soft reset operation.*
0 WAKE_OUT_EN	WAKE power state output enable 0 (default): The device does not signal the WAKE operating mode on the INTx output pin. 1: The device signals that it is currently in WAKE mode via the INT1 or INT2 pin. Whenever **SYS_MODE[**sys_mode**]** = 01b, the INT1 or INT2 pin (as selected in INT_PIN_SEL) is held high or low, depending on the setting made in **SENS_CONFIG4[**INT_POL**]**. The logic state is maintained as long as the device remains in WAKE mode. When the device leaves WAKE mode and enters SLEEP or EXT_TRIG mode, the selected interrupt pin assumes the opposite logic state. ***Note:*** *If the host system is utilizing the WAKE_OUT function to control an external load switch or LDO enable signal, other enabled interrupts should not be mapped to the same pin that is assigned to the WAKE_OUT function in order to prevent unintended operation of the load switch or LDO.*

15.22 INT_PIN_SEL register (address 21h)

This register may be used to control the routing of event flags to either the INT1 or INT2 output pins.

Notes:

- *When the INT2 pin is configured for the external trigger function, for example, when **SENS_CONFIG4[**INT2_FUNC**]** = 1, a logic '1' value in any of these bit fields is ignored.*
- *When BT_MODE = V_{DD}, the only interrupt that may be mapped to the INT2/BOOT_OUT pin is the SRC_BOOT interrupt; setting any of the other bits in this register to '1' effectively unroutes the respective interrupt source from both the INT1 and INT2 pins.*

Table 73. INT_PIN_SEL register (address 21h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	DRDY_INT2	BUF_INT2	SDCD_OT_INT2	SDCD_WT_INT2	ORIENT_INT2	ASLP_INT2	BOOT_INT2	WAKE_OUT_INT2
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 74. INT_PIN_SEL register (address 21h) bit description

Field	Description
7 DRDY_INT2	Data-ready interrupt routing 0: If data-ready interrupt routing is enabled, the interrupt signal is routed to INT1 pin. 1: If data-ready interrupt routing is enabled, the interrupt signal is routed to INT2 pin.
6 BUF_INT2	Output buffer interrupt routing (**BUF_OVF** | **BUF_WMRK** | **BUF_GATE_ERR**): 0: If output buffer interrupt routing is enabled, the interrupt signal is routed to INT1 pin. (default) 1: If output buffer interrupt routing is enabled, the interrupt signal is routed to INT2 pin.
5 SDCD_OT_INT2	SDCD outside of thresholds event interrupt routing 0: If SDCD outside of thresholds event interrupt routing is enabled, the interrupt signal is routed to INT1 pin. 1: If SDCD outside of thresholds event interrupt routing is enabled, the interrupt signal is routed to INT2 pin.
4 SDCD_WT_INT2	SDCD within thresholds event interrupt routing 0: If SDCD within thresholds event interrupt routing is enabled, the interrupt signal is routed to INT1 pin. 1: If SDCD within thresholds event interrupt routing is enabled, the interrupt signal is routed to INT2 pin.
3 ORIENT_INT2	ORIENT event interrupt routing 0: If ORIENT event interrupt routing is enabled, the interrupt signal is routed to INT1 pin. 1: If ORIENT event interrupt routing is enabled, the interrupt signal is routed to INT2 pin.
2 ASLP_INT2	Auto-WAKE/SLEEP event interrupt routing 0: If Auto-WAKE/SLEEP event interrupt routing is enabled, the interrupt signal is routed to INT1 pin. 1: If Auto-WAKE/SLEEP event interrupt routing is enabled, the interrupt signal is routed to INT2 pin.
1 BOOT_INT2	BOOT event interrupt routing If a user operation sets BOOT_INT2 before issuing a soft reset command, the setting is maintained through the reset sequence (the setting is lost if V_{DD} supply is removed). 0: If BOOT event interrupt routing is enabled, the interrupt signal is routed to INT1 pin. 1: If BOOT event interrupt routing is enabled, the interrupt signal is routed to INT2 pin. ***Note:*** *When BT_MODE = V_{DD}, this bit is ignored; the BOOT interrupt is internally mapped to the INT2/BOOT_OUT pin (fixed setting).*
0 WAKE_OUT_INT2	WAKE power state interrupt routing 0: If WAKE power state interrupt routing is enabled, the WAKE power state output is routed to INT1 pin. 1: If WAKE power state interrupt routing is enabled, the WAKE power state output is routed to INT2 pin.

15.23 OFF_X, OFF_Y, OFF_Z registers (addresses 22h to 24h)

Registers 22h to 24h (OFF_X/Y/Z) can be used to realign the zero-*g* position of the X-, Y-, and Z-axes after PCB assembly. The registers are 8 bit, 2's complement providing an offset adjustment range of –128 to 127.

Equation 2 determines the effective offset value in m*g*, set by each of the OFF_X/Y/Z registers. The equation is an X-axis example, with the other axes offsets set in an identical manner.

$$\text{Offset (mg)} = \text{OFF\_X} * (2 * \text{Sensitivity} \left(\frac{\text{mg}}{\text{LSB}}\right)) \quad (2)$$

For example, writing the value +16 (10h) into the OFF_X register in the ±4 *g* FSR results in an effective X-axis offset of 16 LSB * 2 * 1.95 m*g*/LSB = 62.4 m*g*.

Table 75. OFF_X register (addresses 22h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	OFF_X[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 76. OFF_Y register (addresses 23h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	OFF_Y[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 77. OFF_Z register (addresses 24h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	OFF_Z[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15.24 BUF_CONFIG1 register (address 26h)

The BUF_CONFIG1 register controls the output buffer read order, data collection mode and trigger event sources.

Table 78. BUF_CONFIG1 register (address 26h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	BUF_TYPE	BUF_MODE[1:0]		BUF_GATE	TRIG_ SDCD_WT	TRIG_ SDCD_OT	—	TRIG_ ORIENT
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 79. BUF_CONFIG1 register (address 26h) bit description

Field	Description
7 BUF_TYPE	Buffer data read out order: 0: First In First Out (FIFO). Default In FIFO mode, the oldest sample data is read out first, followed by the more recent sample data. 1: First In Last Out (LIFO). In LIFO mode, the newest data sample is read out first, followed by the older sample data. ***Note:*** *It is not possible to change the buffer operating mode without first clearing the* ***SENS_ CONFIG1[****ACTIVE****]*** *and* ***SENS_CONFIG4[****INT2_FUNC****]*** *bits.*

Table 79. BUF_CONFIG1 register (address 26h) bit description*...continued*

Field	Description
6 to 5 BUF_MODE[1:0]	Buffer data collection mode: 00: Buffer is disabled. 01: Stream Mode: buffer always contains the most recent 32 samples when overflowed. The oldest sample data is replaced with new data when the buffer becomes full and a new sample arrives. 10: Stop Mode: buffer stops accepting new samples when full. 11: Trigger mode: The buffer will operate in circular mode until the trigger event occurs, collecting up to **BUF_CONFIG2[**BUF_WMRK[5:0]**]** samples; after a configured trigger event occurs the buffer continues to accept up to (32- **BUF_CONFIG2[**BUF_WMRK[5:0]**]**) samples, set the BUF_OVF flag, and stop collecting further samples. Trigger mode allows acceleration data to be collected both before and after the trigger event, with the maximum number of pre-trigger samples defined by the **BUF_CONFIG2[**BUF_WMRK[5:0]**]** setting. ***Note:*** *The BUF_OVF flag is cleared and the triggered mode re-armed once the host flushes or reads all the buffer contents.* The available trigger sources are the SDCD within- and outside-of-thresholds events, and orientation change event. These trigger sources are enabled in this register via the TRIG_SDCD_WT, TRIG_SDCD_OT, and TRIG_ORIENT bits.
4 BUF_GATE	Output data buffer gate enable: 0: Buffer gate is bypassed (default). Output data buffer is automatically flushed when FXLS8967AF transitions from WAKE to SLEEP or SLEEP to WAKE modes. This operation prevents acceleration data from two different ODRs rates becoming mixed in the output buffer. 1: The Output data buffer input gate is enabled when transitioning from WAKE to SLEEP or SLEEP to WAKE modes; the entire buffer contents must be read out or flushed (**BUF_CONFIG2[**BUF_FLUSH**]** = 1) to allow the further collection of sample data. Any new samples that arrive before the buffer has been read out or flushed are discarded, and the BUF_GATE_ERR bit in the **SYS_MODE** register is asserted. **SYS_MODE[**BUF_GATE_CNT**]** maintains a count of the number of samples discarded since the BUF_GATE_ERR flag was asserted. Although FXLS8967AF still transitions from WAKE to SLEEP or SLEEP to WAKE, the contents of the FIFO buffer are preserved, and any new data samples are not stored in the buffer until it is either emptied of flushed by the host application. ***Notes:*** • *The BUF_GATE_ERR flag remains asserted as long as the buffer remains un-emptied.* • *When triggered buffer mode (BUF_MODE = 11b) is selected and **ASLP_COUNT** ≥ 1, the BUF_GATE setting is ignored.* • *The BUF_GATE bit in 1: Trigger source is enabled, when set, holds the last data set stored in the buffer before transitioning to the SLEEP or WAKE modes. After the buffer is flushed, FXLS8967AF will start accepting new sample data into the buffer at the current operating mode ODR.*
3 TRIG_SDCD_WT	SDCD within thresholds event buffer trigger enable: 0: Trigger source is disabled (default). 1: Trigger source is enabled
2 TRIG_SDCD_OT	SDCD outside of thresholds event buffer trigger enable: 0: Trigger source is disabled (default). 1: Trigger source is enabled
0 TRIG_ORIENT	Orientation change event buffer trigger enable: 0: Trigger source is disabled (default). 1: Trigger source is enabled

The buffer contents are flushed whenever the buffer is disabled (by setting BUF_MODE = 00b), when **BUF_CONFIG2[**BUF_FLUSH**]** is set, or after an automatic power mode change when transitioning from WAKE-to-SLEEP or SLEEP-to-WAKE with **BUF_CONFIG1[**BUF_GATE**]** = 0. The buffer contents are also automatically flushed on a

transition from STANDBY to ACTIVE or STANDBY to EXT_TRIG mode. The buffer may be prevented from being flushed when transitioning from WAKE-to-SLEEP or SLEEP-to-WAKE by setting **BUF_CONFIG1[**BUF_GATE**]** = 1.

Disabling the buffer clears the **BUF_STATUS[**BUF_OVF**]** and **BUF_STATUS[**BUF_WMRK**]** event flags. Disabling the buffer also clears the **BUF_STATUS[**BUF_CNT**]** field. The **SYS_MODE[**BUF_GATE_ERR**]** and **SYS_MODE[**buf_gate_cnt**]** fields are also reset when the buffer is disabled, flushed, or when the host reads out all the content.

Notes for using triggered operating mode with Auto-WAKE/SLEEP mode enabled:

1. When BUF_MODE = 11b, **ASLP_COUNT** ≥ 1, and the ACTIVE bit is set, FXLS8967AF immediately enters the WAKE mode. After **ASLP_COUNT** ODR periods, the buffer is flushed and the part enters SLEEP mode. The buffer collects up to **BUF_CONFIG2[**BUF_WMRK**]** samples at the SLEEP mode ODR before the trigger event occurs (in stream mode).
2. After the trigger event, FXLS8967AF enters WAKE mode and remain there regardless of the setting made in **ASLP_COUNT**, ignore any subsequent triggers, and collects (32 - BUF_WMRK[5:0]) samples at the WAKE mode ODR, set the BUF_OVF flag, and cease collecting more data until the host flushes the buffer or reads out all of the contents. Once the buffer is emptied or flushed, the triggered mode is re-armed, but FXLS8967AF must first re-enter SLEEP mode (which will happen after **ASLP_COUNT** *WAKE* ODR periods) before a second set of data can be collected.
3. The **BUF_CONFIG1[**BUF_GATE**]** setting is ignored and has no effect. The buffer contents are automatically flushed when FXLS8967AF transitions from WAKE to SLEEP.
4. The interrupt events that prevent FXLS8967AF from entering SLEEP mode also prevents the operation of the triggered mode (which requires FXLS8967AF to first enter the SLEEP mode).

15.25 BUF_CONFIG2 register (address 27h)

Table 80. BUF_CONFIG2 register (address 27h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	BUF_ FLUSH	WAKE_ SRC_BUF	BUF_WMRK[5:0]					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 81. BUF_CONFIG2 register (address 27h) bit description

Field	Description
7 BUF_FLUSH	Buffer flush enable: 0: No pending buffer flush operation, or buffer flush completed 1: Buffer flush enable: all buffer contents and related event flags are cleared. The **SYS_ MODE[**BUF_GATE_ERR**]** and **SYS_MODE[**BUF_GATE_CNT[4:0]**]** fields are also cleared. The BUF_FLUSH bit is self-cleared within one internal clock cycle, and as such is not observable in a logic high state through the I^2C or SPI interfaces.

Table 81. BUF_CONFIG2 register (address 27h) bit description*...continued*

Field	Description
6 WAKE_SRC_BUF	Buffer WAKE-to-SLEEP transition source enable: 0: (BUF_WMRK | BUF_OVF) event flag condition is ignored by the auto-WAKE/SLEEP function (default). 1: (BUF_WMRK | BUF_OVF) event flag condition is used by the auto-WAKE/SLEEP function. FXLS8967AF enters SLEEP mode if the host system does not clear any of these flags before the auto-sleep timer expires (the **ASLP_COUNT** register sets the period). If the host clears the BUF_WMRK and BUF_OVF flags by flushing or reading out the buffered data (one or more samples), the auto-sleep timer resets and FXLS8967AF remains in the WAKE mode, regardless of the setting made in **INT_EN[**BUF_EN**]**. ***Note:** The WAKE_SRC_BUF setting is only relevant when **BUF_CONFIG1[**BUF_MODE**]** = 01b (Stream mode) or 10b (Stop mode).*
5 to 0 BUF_WMRK[5:0]	Buffer sample count watermark: This field sets the minimum number of buffer samples required to trigger a watermark interrupt. A buffer watermark event flag **BUF_STATUS[**BUF_WMRK**]** is raised whenever **BUF_STATUS[**BUF_CNT**]** ≥ **BUF_CONFIG2[**BUF_WMRK[5:0]**]**. Setting BUF_WMRK = 0 disables the buffer watermark event flag generation. This field is also used to set the maximum number of pre-trigger samples to collect in triggered operating mode when **BUF_CONFIG1[**BUF_MODE**]** = 11b.

15.26 ORIENT_STATUS register (address 28h)

The ORIENT_STATUS register is used to determine the status of an Orientation change event, which is signaled when **INT_STATUS[**SRC_ORIENT**]** = 1. For information on the physical device orientations that correspond to the portrait up, portrait down, landscape left, landscape right, back, and front orientation states, see Section 6.3.

Table 82. ORIENT_STATUS register (address 28h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	NEW_ORIENT	LO	—			LAPO[1:0]		BAFRO
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 83. ORIENT_STATUS register (address 28h) bit description

Field	Description
7 NEW_ORIENT	Orientation status change flag 0: No change in orientation detected 1: BAFRO and/or LAPO and/or Z-tilt lockout value has changed ***Notes:*** • *The NEW_ORIENT bit is set to 1 after the first orientation detection after a Standby to Active transition and whenever a change in LO, BAFRO, or LAPO status occurs. The NEW_ORIENT bit is cleared anytime the ORIENT_STATUS register is read.* • *The Auto-WAKE/SLEEP timer is reset (cleared) on the rising edge of this flag.*

Table 83. ORIENT_STATUS register (address 28h) bit description*...continued*

Field	Description
6 LO	Z-tilt angle lockout 0: Lockout condition has not been detected. 1: Z-tilt lockout trip angle has been exceeded. Lockout condition has been detected. ***Note:*** *The LO bit continues to update with orientation changes even after the* ***NEW_ORIENT*** *flag is set.*
2 to 1 LAPO[1:0]	Landscape/Portrait orientation 00: Portrait up: The device is oriented vertically in the upward direction. 01: Portrait down: The device is oriented vertically in the downward direction. 10: Landscape right: The device is oriented horizontally to the right. 11: Landscape left: The device is oriented horizontally to the left. ***Note:*** *The* ***LAPO[****1:0****]*** *field continues to update with orientation changes even after the* ***NEW_ORIENT*** *flag is set.*
0 BAFRO	Back or front orientation 0: Front: The device is in the front-facing orientation. 1: Back: The device is in the back-facing orientation. ***Note:*** *The* ***BAFRO*** *bit continues to update with orientation changes even after the* ***NEW_ORIENT*** *flag is set.*

Notes:

- *The BAFRO and LAPO fields are reset to 0 after a POR or soft reset event. These bits are also automatically cleared after a transition from STANDBY to ACTIVE or STANDBY to EXT_TRIG modes.*
- *The current orientation is locked if the absolute value of the acceleration experienced on any of the three axes is greater than 1.25 g.*

15.27 ORIENT_CONFIG register (address 29h)

This register is used to enable the orientation detection function and set the behavior of the orientation transition debounce counter.

Table 84. ORIENT_CONFIG register (address 29h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	ORIENT_ DBCNTM	ORIENT_ ENABLE	—					
Reset	1	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 85. ORIENT_CONFIG register (address 29h) bit description

Field	Description
7 ORIENT_DBCNTM	Orientation debounce counter mode selection 0: Orientation debounce counter is decremented whenever the current orientation is different than the previous one. 1: Orientation debounce counter is cleared whenever the current orientation is different than the previous one.

Table 85. ORIENT_CONFIG register (address 29h) bit description*...continued*

Field	Description
6 ORIENT_ENABLE	Orientation detection function enable 0 (default): Orientation detection function is disabled. 1: Orientation detection function is enabled.

15.28 ORIENT_DBCOUNT register (address 2Ah)

The **ORIENT_DBCOUNT** register sets the debounce count used for validating an orientation state change. The selected ODR in LPM and HPM modes, and the effective ODR when operating in FPM determine the debounce counter period. Calculate the minimum debounce latency time by ODR^{-1} * **ORIENT_DBCOUNT**[7:0]. For example, with an ODR of 100 Hz and debounce count value of 10, the new orientation must be maintained for 100 ms before it is recognized as a valid orientation and **ORIENT_STATUS[**NEW_ORIENT**]** is asserted. A transition from Standby to Active, a transition from Active to Standby, or a change in the auto-WAKE/SLEEP mode resets the internal orientation debounce counter.

Table 86. ORIENT_DBCOUNT register (address 2Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	ORIENT_DBCOUNT[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 87. ORIENT_DBCOUNT register (address 2Ah) bit description

Field	Description
7 to 0 ORIENT_ DBCOUNT[7:0]	8-bit unsigned orientation debounce counter value A new orientation must be maintained for the minimum number of ODR periods specified in order for the orientation to be considered valid before asserting the **ORIENT_STATUS[**NEW_ORIENT**]** event flag. **ORIENT_CONFIG[**ORIENT_DBCNTM**]** controls the counter behavior. The selected ODR in LPM and HPM modes and the effective ODR when operating in FPM determines the debounce counter period. Calculate the minimum debounce latency time by: Debounce_time = (ODR^{-1} * ORIENT_DBCOUNT) ***Note:*** *If the applied acceleration is greater than 1.25 g on any axis, the debounce counter is held at the current value (frozen).*

15.29 ORIENT_BF_ZCOMP register (address 2Bh)

Orientation back/front and Z-tilt angle compensation register

Table 88. ORIENT_BF_ZCOMP register (address 2Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	ORIENT_BKFR[1:0]		—			ORIENT_ZLOCK[2:0]		
Reset	0	1	0	0	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 89. ORIENT_BF_ZCOMP register (address 2Bh) bit description

Field	Description
7 to 6 ORIENT_ BKFR[1:0]	Back-up/Front-up trip angle threshold Default: 01b; Step size is ~5°/ LSB. Range: ±65° to ±80°. Default value of ±75°
2 to 0 ORIENT_ ZLOCK[2:0]	Z-lockout angle threshold Range of ~13° to 44°. Step size is ~4°. Default value of 28.1°

Table 90. ORIENT_ZLOCK lockout angles

ORIENT_ ZLOCK[2:0]	Resultant angle (min) for positions between Landscape and Portrait	Resultant angle (max) for ideal Landscape or Portrait
000	13.6°	14.5°
001	17.1°	18.2°
010	20.7°	22.0°
011	24.4°	25.9°
100	28.1°	30.0°
101	32.0°	34.2°
110	36.1°	38.7°
111	40.4°	43.4°

Table 91. ORIENT Back/Front orientation transition angle definitions

BKFR[1:0]	Back-to-Front Transition	Front-to-Back Transition
00	Z < 80° or Z > 280°	Z > 100° and Z < 260°
01	Z < 75° or Z > 285°	Z > 105° and Z < 255°
10	Z < 70° or Z > 290°	Z > 110° and Z < 250°
11	Z < 65° or Z > 295°	Z > 115° and Z < 245°

15.30 ORIENT_THS register (address 2Ch)

Orientation change trip thresholds configuration

Table 92. ORIENT_THS register (address 2Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	ORIENT_THS[4:0]					ORIENT_HYS[2:0]		
Reset	1	0	0	0	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 93. Orientation change trip angles look-up table

ORIENT_THS[4:0] value	Threshold angle (approx.)
00h	0.0°
01h	1.8°
02h	3.8°
03h	5.9°
04h	8.1°
05h	10.5°
06h	13.0°
07h	15.6°
08h	18.4°
09h	21.4°
0Ah	24.4°
0Bh	27.6°
0Ch	31.0°
0Dh	34.4°
0Eh	37.9°
0Fh	41.4°
10h	45.0°
11h	48.6°
12h	52.1°
13h	55.6°
14h	59.0°
15h	62.4°
16h	65.6°
17h	68.6°
18h	71.6°
19h	74.4°
1Ah	77.0°
1Bh	79.5°
1Ch	81.9°
1Dh	84.1°
1Eh	86.2°
1Fh	88.2°

Table 94. Resultant trip angle (threshold angle ± hysteresis angle)

ORIENT_HYS[2:0]	Landscape-to-Portrait trip angle	Portrait-to-Landscape trip angle
0	45°	45°
1	49°	41°
2	52°	38°
3	56°	34°
4	59°	31°
5	62°	28°
6	66°	24°
7	69°	21°

Note: *In Table 94, the default threshold angle of 45° is considered for calculating the resultant trip angle.*

Table 95. Orientation change ideal orientation angle definitions

Orientation	X/Y axis g-levels
PU	y ~ –1 *g*, x ~ 0
PD	y ~ +1 *g*, x ~ 0
LR	y ~ 0, x ~ +1 *g*
LL	y ~ 0, x ~ –1 *g*

15.31 Sensor Data Change Detection (SDCD) registers

The Sensor Data Change Detection (SDCD) function is an inertial event detection function available to assist host software algorithms in detecting various inertial events such as motion/no-motion, high-*g*/low-*g*, tap/double tap, and transient acceleration events.

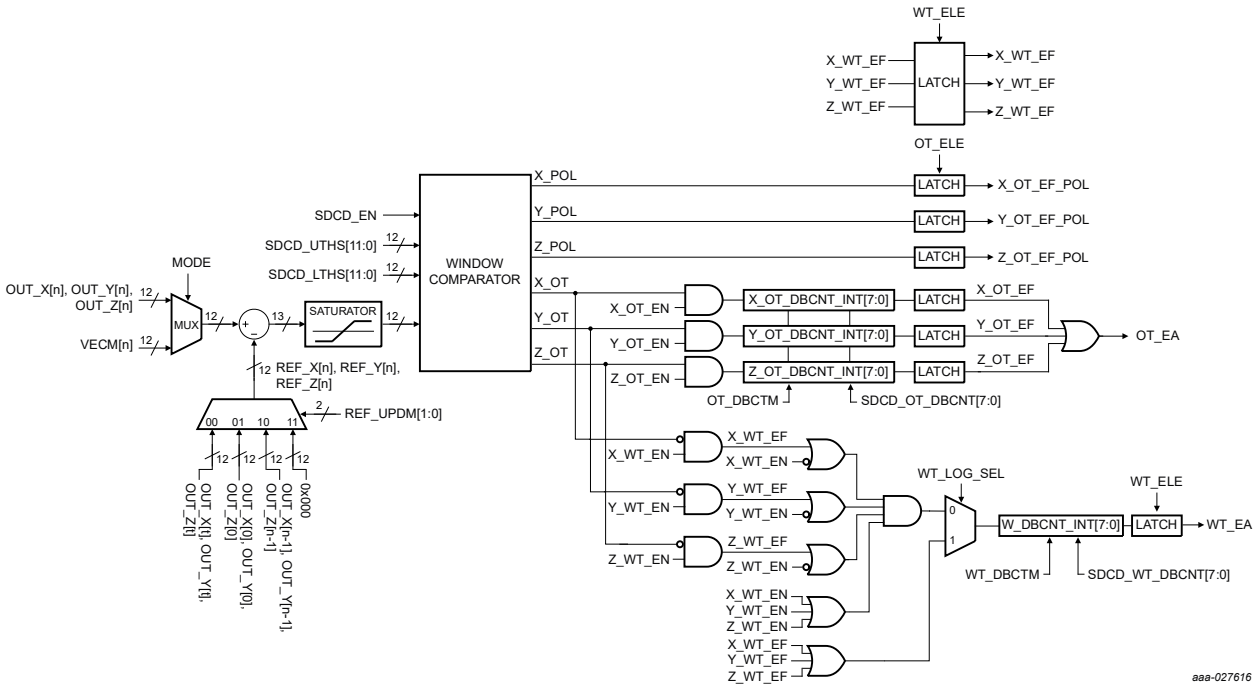


Figure 17. SDCD Function Block Diagram

15.31.1 SDCD_INT_SRC1 register (address 2Dh)

This register contains the SDCD outside-of-thresholds event status flags. If mapped to one of the INT1 or INT2 pins, the OT_EA flag may be used to signal interrupts to a host processor.

Table 96. SDCD_INT_SRC1 register (address 2Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	OT_EA	—	X_OT_EF	X_OT_POL	Y_OT_EF	Y_OT_POL	Z_OT_EF	Z_OT_POL
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 97. SDCD_INT_SRC1 register (address 2Dh) bit description

Field	Description
7 OT_EA	SDCD outside-of-thresholds event active flag 0 (default): Event flag has not been asserted; the data for all enabled axes is within the window defined by **SDCD_UTHS** and **SDCD_LTHS** registers. 1: One or more of the enabled axes sensor data (absolute mode) or deltas (relative mode) sits on or outside of (for example, (data or delta) ≤ **SDCD_LTHS** or (data or delta) ≥ **SDCD_UTHS**) the upper or lower thresholds specified in the **SDCD_UTHS** and **SDCD_LTHS** registers. The OT_EA flag is set whenever (X_OT_EF | Y_OT_EF | Z_OT_EF**)** evaluates to true for a number of ODR periods ≥ **SDCD_OT_DBCNT**. ***Notes:*** • *The axes selected for participation in the over thresholds condition evaluation are enabled via the X/Y/Z_OT_EN bits in the **SDCD_CONFIG1** register. If none of the X/Y/Z_OT_EN bits are set, then the SDCD_OT function is effectively disabled.* • *When SENS_CONFIG4[WAKE_SDCD_OT] = 1, the Auto-WAKE/SLEEP timer is reset on every ODR cycle when the OT_EA flag is asserted (set), which prevents the device from transitioning into SLEEP mode. This flag must be de-asserted (cleared) in order for FXLS8967AF to transition to SLEEP mode.*
5 X_OT_EF	X-axis data or delta-outside-of-upper-and-lower-thresholds event flag; enabled if X_OT_EN = 1 0: X-axis data or delta is < **SDCD_UTHS** value and > **SDCD_LTHS** value. 1: X-axis data or delta is either ≥ **SDCD_UTHS** value or ≤ **SDCD_LTHS** value; the X_OT_POL flag may be used to determine which threshold has been met or crossed.
4 X_OT_POL[1][2]	X-axis outside-of-thresholds polarity flag 0: X-axis data or delta was ≤ lower threshold value 1: X-axis data or delta was ≥ upper threshold value
3 Y_OT_EF	Y-axis data or delta-outside-of-upper-and-lower-thresholds event flag; enabled if Y_OT_EN = 1 0: Y-axis data or delta is < **SDCD_UTHS** value and > **SDCD_LTHS** value. 1: Y-axis data or delta is either ≥ **SDCD_UTHS** value or ≤ **SDCD_LTHS** value; the Y_OT_POL flag may be used to determine which threshold has been met or crossed.
2 Y_OT_POL[1][2]	Y-axis outside-of-thresholds polarity flag 0: Y-axis data or delta was equal to or below lower threshold value 1: Y-axis data or delta was equal to or above upper threshold value
1 Z_OT_EF[1][2]	Z-axis data or delta-outside-of-upper-and-lower-thresholds event flag; enabled if Z_OT_EN = 1 0: Z-axis data or delta is < **SDCD_UTHS** value and > **SDCD_LTHS** value 1: Z-axis data or delta is either ≥ **SDCD_UTHS** value or ≤ **SDCD_LTHS** value; the Z_OT_POL flag may be used to determine which threshold has been met or crossed
0 Z_OT_POL	Z-axis outside-of-thresholds polarity flag 0: Z-axis data or delta was equal to or below lower threshold value 1: Z-axis data or delta was equal to or above upper threshold value

[1] This flag is only meaningful if X/Y/Z_OT_EF = 1; their individual states are latched when the X/Y/Z_OT_EF flags are set, regardless of the state of SDCD_CONFIG1[OT_ELE].

[2] When SDCD_CONFIG1[OT_ELE] = 0, these flags are updated when X/Y/Z_OT_EF = 1 and the SDCD_OT_DBCNT value is reached.

15.31.2 SDCD_INT_SRC2 register (address 2Eh)

This register contains the SDCD within-thresholds event status flags. The WT_EA flag may be used to signal interrupts to a host processor are mapped to one of the INT1 or INT2 pins.

Table 98. SDCD_INT_SRC2 register (address 2Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	WT_EA	—	X_WT_EF	—	Y_WT_EF	—	Z_WT_EF	—
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 99. SDCD_INT_SRC2 register (address 2Eh) bit description

Field	Description
7 WT_EA	SDCD within-thresholds event active flag 0 (default): Event flag has not been asserted; none of the input data (absolute mode) or deltas (relative mode) for the enabled axes is within the window defined by the **SDCD_UTHS** and **SDCD_LTHS** registers. 1: All, or at least one of, (depending on the LOGIC function selected in **SDCD_CONFIG2[**WT_LOG_SEL**]**) the enabled axes sensor data (absolute mode) or deltas (relative mode) sits within both the upper and lower thresholds specified in the **SDCD_UTHS** and **SDCD_LTHS** registers (for example, > **SDCD_LTHS**, and < **SDCD_UTHS**). This flag is set whenever the condition is true for a number of ODR cycles ≥ **SDCD_WT_DBCNT**. ***Notes:*** • *The axes selected for participation in the within thresholds condition evaluation are enabled via the X/Y/Z_WT_EN bits in the **SDCD_CONFIG1** register. The logic mode for the function is set in the **SDCD_CONFIG2** register. If none of the X/Y/Z_WT_EN bits are set then the SDCD_WT function is effectively disabled.* • *When SENS_CONFIG4[WAKE_SDCD_WT] = 1, the Auto-WAKE/SLEEP timer is reset on every ODR cycle when the WT_EA flag is asserted (set), which prevents the device from transitioning into SLEEP mode. This flag must be de-asserted (cleared) in order for FXLS8967AF to transition to SLEEP mode.*
5 X_WT_EF	X-axis data or delta inside of upper and lower thresholds event flag; This flag is only valid if X_WT_EN = 1: 0: X-axis data or delta is ≥ **SDCD_UTHS** value or ≤ **SDCD_LTHS** value. 1: X-axis data or delta is < **SDCD_UTHS** and > **SDCD_LTHS** value. ***Notes:*** • *The **SDCD_CONFIG1[**WT_ELE**]** bit determines the behavior of this bit. If WT_ELE = 1, the flag is latched when WT_EA goes high, and remains set until it is cleared by reading the **SDCD_INT_SRC2** register. If the host wishes to know the state of this event flag, it must be read prior to reading the **SDCD_INT_SRC2** register.* • *If WT_ELE = 0, the X/Y/Z_WT_EF flags are updated if WT_EA = 1 and the SDCD_WT_DBCNT value is reached. If WT_ELE = 0, the X/Y/Z_WT_EF flags are updated even if WT_EA = 0 when the SDCD_WT_DBCNT value is set to 0.*
3 Y_WT_EF	Y-axis data or delta inside of upper and lower thresholds event flag; This flag is only valid if Y_WT_EN = 1: 0: Y-axis data or delta is ≥ **SDCD_UTHS** value or ≤ **SDCD_LTHS** value. 1: Y-axis data or delta is < **SDCD_UTHS** and > **SDCD_LTHS** value. ***Notes:*** • *The **SDCD_CONFIG1[**WT_ELE**]** bit determines the behavior of this bit. If WT_ELE = 1, the flag is latched when WT_EA goes high, and remains set until it is cleared by reading the **SDCD_INT_SRC2** register. If the host wishes to know the state of this event flag, it must be read prior to reading the **SDCD_INT_SRC2** register.* • *If WT_ELE = 0, the X/Y/Z_WT_EF flags are updated if WT_EA = 1 and the SDCD_WT_DBCNT value is reached. If WT_ELE = 0, the X/Y/Z_WT_EF flags are updated even if WT_EA = 0 when the SDCD_WT_DBCNT value is set to 0.*

Table 99. SDCD_INT_SRC2 register (address 2Eh) bit description*...continued*

Field	Description
1 Z_WT_EF	Z-axis data or delta inside of upper and lower thresholds event flag; This flag is only valid if Z_WT_EN = 1: 0: Z-axis data or delta is ≥ **SDCD_UTHS** value or ≤ **SDCD_LTHS** value. 1: Z-axis data or delta is < **SDCD_UTHS** and > **SDCD_LTHS** value. ***Notes:*** • *The **SDCD_CONFIG1[**WT_ELE**]** bit determines the behavior of this bit. If WT_ELE = 1, the flag is latched when WT_EA goes high, and remains set until it is cleared by reading the **SDCD_INT_SRC2** register. If the host wishes to know the state of this event flag, it must be read prior to reading the **SDCD_INT_SRC2** register.* • *If WT_ELE = 0, the X/Y/Z_WT_EF flags are updated if WT_EA = 1 and the SDCD_WT_DBCNT value is reached. If WT_ELE = 0, the X/Y/Z_WT_EF flags are updated even if WT_EA = 0 when the SDCD_WT_DBCNT value is set to 0.*

15.31.3 SDCD_CONFIG1 register (address 2Fh)

Table 100. SDCD_CONFIG1 register (address 2Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	OT_ELE	WT_ELE	X_OT_EN	Y_OT_EN	Z_OT_EN	X_WT_EN	Y_WT_EN	Z_WT_EN
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	0	0	1	1	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 101. SDCD_CONFIG1 register (address 2Fh) bit description

Field	Description
7 OT_ELE	SDCD outside-of-thresholds event latch 0 (default): Outside of thresholds event flag latching is disabled. 1: Outside of thresholds event flag latching is enabled. With outside-of-thresholds event latching enabled, the X/Y/Z_OT_EF flags can only be cleared by reading the **SDCD_INT_SRC1** register. When OT_ELE is set, the outside-of-thresholds event condition (OT_EA) flag is only asserted when the event condition transitions from False to True. For example, once the OT_EA flag is set, the event condition must become False before a subsequent True event is recognized. With outside-of-thresholds event latching disabled, the X/Y/Z_OT_EF flags are updated in real time and may be cleared by the function prior to the host system reading **SDCD_INT_SRC1** if the event condition becomes false before the read occurs.
6 WT_ELE	SDCD within-thresholds event latch 0 (default): Within thresholds event flag latching is disabled. 1: Within thresholds event flag latching is enabled. With within-thresholds event latching enabled, the X/Y/Z_WT_EF flags can only be cleared by reading the **SDCD_INT_SRC2** register. When within-thresholds event latching is disabled, the X/Y/Z_WT_EF flags are updated in real time and may be cleared by the function prior to the host system reading the **SDCD_INT_SRC2** register, if the event condition becomes false before the read occurs. When WT_ELE is set, the within-thresholds event condition (WT_EA) flag is only asserted when the event condition transitions from False to True. For example, once the WT_EA flag is set, the event condition must become False before a subsequent True event will be recognized
5 X_OT_EN	SDCD function X-axis outside-of-thresholds condition 0: X-axis data or delta is not used in the outside of thresholds condition evaluation. 1: X-axis data or delta is used in the outside of thresholds condition evaluation.

Table 101. SDCD_CONFIG1 register (address 2Fh) bit description*...continued*

Field	Description
4 Y_OT_EN	SDCD function Y-axis outside-of-thresholds condition 0: Y-axis data or delta is not used in the outside of thresholds condition evaluation. 1: Y-axis data or delta is used in the outside of thresholds condition evaluation.
3 Z_OT_EN	SDCD function Z-axis outside-of-thresholds condition 0: Z-axis data or delta is not used in the outside of thresholds condition evaluation. 1: Z-axis data or delta is used in the outside of thresholds condition evaluation.
2 X_WT_EN	SDCD function X-axis within-thresholds condition 0: X-axis data or delta is not used in the within thresholds condition evaluation. 1: X-axis data or delta is used in the within thresholds condition evaluation.
1 Y_WT_EN	SDCD function Y-axis within-thresholds condition 0: Y-axis data or delta is not used in the within thresholds condition evaluation. 1: Y-axis data or delta is used in the within thresholds condition evaluation.
0 Z_WT_EN	SDCD function Z-axis within-thresholds condition 0: Z-axis data or delta is not used in the within thresholds condition evaluation. 1: Z-axis data or delta is used in the within thresholds condition evaluation.

15.31.4 SDCD_CONFIG2 register (address 30h)

Table 102. SDCD_CONFIG2 register (address 30h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	SDCD_EN	REF_UPDM[1:0]		OT_ DBCTM	WT_ DBCTM	WT_ LOG_SEL	MODE	REF_UPD
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	1	1	0	1	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 103. SDCD_CONFIG2 register (address 30h) bit description

Field	Description
7 SDCD_EN	SDCD function 0 (default after a POR or soft reset event when BT_MODE = GND): SDCD function is disabled. All clocks and power for the function are turned off. 1 (default after a POR or soft reset event when BT_MODE = V_{DD} and MOT_DET = 1): SDCD function is enabled. When this bit is set, the 12-bit reference values (**REF_X/Y/Z**) are initialized per the settings made in REF_UPDM[1:0].

Table 103. SDCD_CONFIG2 register (address 30h) bit description*...continued*

Field	Description
6 to 5 REF_UPDM	SDCD internal reference values update mode 00b: The function stores the first 12-bit X/Y/Z decimated and trimmed input data (OUT_X/Y/Z[n=0]) as the internal REF_X/Y/Z values after the function is enabled (SDCD_EN is set to 1). The REF_X/Y/Z values are updated with the current 12-bit X/Y/Z decimated input data (OUT_X/Y/Z[n]) at the time the SDCD_OT_EA flag transitions from false to true. 01b: The function stores the first decimated and trimmed X/Y/Z acceleration input data (OUT_X/Y/Z[n=0]) as the internal REF_X/Y/Z values when the SDCD function is enabled; the REF_X/Y/Z values are then held constant and never updated until the SDCD function is disabled and subsequently reenabled, or asynchronously when the host sets the REF_UPD bit. 10b: The function updates the SDCD_REF_X/Y/Z values with the current decimated and trimmed X/Y/Z acceleration input data after the function evaluation. This operation allows for acceleration slope detection with Data(n) to Data(n–1) always used as the input to the window comparator. 11b: The function uses a fixed value of 0 for each of the SDCD_REF_X/Y/Z registers, making the function operate in absolute comparison mode.
4 OT_DBCTM	SDCD outside-of-threshold event debounce counter behavior 0 (default): Debounce counter decrements by 1 when the current outside of thresholds result for the enabled axes is false. In this mode, the debounce counter de-bounces the outside of thresholds event in both directions, meaning that once the event flag has been set (after SDCD_OT_DBCNT ODR periods with the condition true), the condition must also remain false for at least SDCD_OT_DBCNT + 1 consecutive ODR periods before the next event detection cycle can begin. 1: Debounce counter is cleared whenever the current outside of thresholds result for the enabled axes is false.
3 WT_DBCTM	SDCD within-thresholds event debounce counter behavior 0 (default): Debounce counter decrements by 1 when the current within thresholds result for the enabled axes is false. In this mode, the debounce counter de-bounces the event in both directions, meaning that once the event flag has been set (after SDCD_WT_DBCNT ODR periods with the condition true), the condition must also remain false for at least SDCD_WT_DBCNT + 1 consecutive ODR periods before the next event detection cycle can begin. 1: Debounce counter is cleared whenever the SDCD within thresholds result for the enabled axes is false.
2 WT_LOG_SEL	SDCD within-thresholds event logic selection 0 (default): Function uses the logical AND of the enabled axes. 1: Function uses the logical OR of the enabled axes.
1 MODE	SDCD input data mode 0 (default): Function uses X, Y, Z acceleration data for the window comparison. 1: Function uses Vector magnitude data for the window comparison on the X-axis channel only; all other SDCD channels are disabled and ignored by the function. ***Note:*** *The SENS_CONFIG5[VECM_EN] bit must also be set in order for the SDCD function to operate correctly when MODE is set to 1.*
0 REF_UPD	SDCD synchronous X/Y/Z reference values update bit 0: No reference update pending or reference update has completed. 1: Triggers a synchronous update of the internal X/Y/Z reference registers. When the REF_UPD bit is set, it forces a synchronous update of the internal REF_X/Y/Z registers. If REF_UPDM[1:0] = 11b (absolute mode), no update occurs and the REF_X/Y/Z values remain fixed at 000h. The actual update of the internal reference values with the X/Y/Z acceleration data may be delayed by up to 1 ODR period after this bit is set. See Figure 18 for further details. ***Notes:*** • *This bit is self-cleared after the REF_X/Y/Z registers are updated. The host may not be able to observe a value of '1' as the operation can complete before the next I^2C or SPI read cycle occurs.* • *This bit can be written at any time in either Active or Standby mode.*

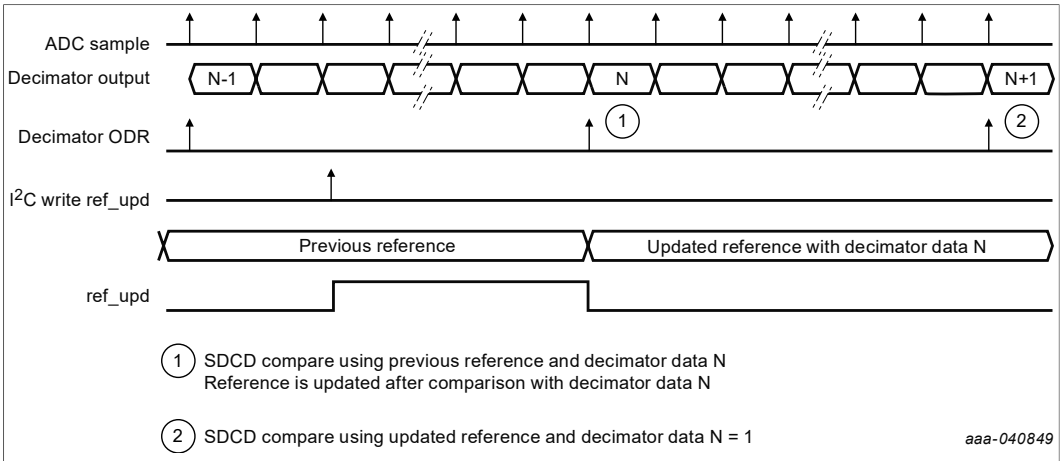


Figure 18. SDCD REF_UPD timing diagram

15.31.5 SDCD_OT_DBCNT register (address 31h)

Debounce count threshold register for SDCD outside-of-thresholds condition event detection.

The timer count period is equal to the selected ODR period in LPM and HPM modes, and to the effective ODR period (measurement + idle time) in FPM.

This register sets the minimum number of debounce counts needed to recognize the SDCD outside-of-threshold function event condition as true.

A transition from Standby to Active, Active to Standby, or Auto-WAKE/SLEEP mode change resets the internal counter.

Table 104. SDCD_OT_DBCNT register (address 31h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	SDCD_OT_DBCNT[7:0]							
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 105. SDCD_OT_DBCNT register (address 31h) bit description

Field	Description
7 to 0 SDCD_OT_ DBCNT[7:0]	This value defines the minimum number of debounce counts required for the detection of an outside-of-thresholds condition. The OT_DBCNTM bit determines the behavior of the counter when the condition of interest is false. The time step for the counter is the same as the selected ODR period (or effective ODR period in FPM).

15.31.6 SDCD_WT_DBCNT register (address 32h)

Debounce count threshold register for SDCD within-thresholds condition event detection.

The timer count period is equal to the selected ODR period in LPM and HPM modes, and to the effective ODR period (measurement + idle time) in FPM.

This register sets the minimum number of debounce counts needed to recognize the SDCD within-threshold condition as true.

A transition from Standby to Active, Active to Standby, or a change in an Auto-WAKE/SLEEP mode change resets the internal counter.

Table 106. SDCD_WT_DBCNT register (address 32h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	SDCD_WT_DBCNT[7:0]							
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 107. SDCD_WT_DBCNT register (address 32h) bit description

Field	Description
7 to 0 SDCD_WT_DBCNT[7:0]	The SDCD_WT_DBCNT value defines the minimum number of debounce sample counts required for the detection of an SDCD_WT condition event. The WT_DBCNTM bit determines the behavior of the counter when the condition of interest is momentarily not true. The time step for the counter is the same as the selected ODR period (or effective ODR period in FPM).

15.31.7 SDCD_LTHS_LSB register (address 33h)

Sensor Data Change Detection function 12-bit 2's complement lower threshold least significant byte. **SDCD_LTHS[**11:0**]** must always be set to a lower value than **SDCD_UTHS[**11:0**]** to ensure that the SDCD circuit functions correctly and produces meaningful results.

The scaling for this register is always the same as the selected FSR sensitivity. See Section 9 for the sensitivity values corresponding to each of the selectable FSRs.

Table 108. SDCD_LTHS_LSB register (address 33h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	SDCD_LTHS[7:0]							
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	1	1	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 109. SDCD_LTHS_LSB register (address 33h) bit description

Field	Description
7 to 0 SDCD_LTHS[7:0]	LSB of the signed 12-bit 2's complement lower threshold value.

15.31.8 SDCD_LTHS_MSB register (address 34h)

Sensor Data Change Detection function 12-bit 2's complement lower threshold most significant byte (nibble). **SDCD_LTHS[**11:0**]** must always be set to a lower value than

SDCD_UTHS[11:0**]** to ensure that the SDCD circuit functions correctly and produces meaningful results.

The scaling for this register is always the same as the selected FSR sensitivity. See Section 9 for the sensitivity values corresponding to each of the selectable FSRs.

Table 110. SDCD_LTHS_MSB register (address 34h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	SDCD_LTHS[11:8]			
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	0	0	0	0	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 111. SDCD_LTHS_MSB register (address 34h) bit description

Field	Description
3 to 0 SDCD_LTHS[11:8]	MSB (nibble) of the signed 12-bit 2's complement lower-threshold value

15.31.9 SDCD_UTHS_LSB register (address 35h)

Sensor Data Change Detection function 12-bit 2's complement upper-threshold least significant byte. **SDCD_UTHS[**11:0**]** must always be set to a higher value than **SDCD_LTHS[**11:0**]** to ensure that the SDCD circuit functions correctly and produces meaningful results.

The scaling for this register is the same as the selected FSR sensitivity. See Section 9 for the sensitivity values corresponding to each of the selectable FSRs.

Table 112. SDCD_UTHS_LSB register (address 35h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	SDCD_UTHS[7:0]							
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	0	1	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 113. SDCD_UTHS_LSB register (address 35h) bit description

Field	Description
7 to 0 SDCD_UTHS[7:0]	LSB of the signed 12 bit 2's complement upper-threshold value

15.31.10 SDCD_UTHS_MSB register (address 36h)

Sensor Data Change Detection function 12-bit 2's complement upper-threshold most-significant byte (nibble). **SDCD_UTHS[**11:0**]** must always be set to a higher value than **SDCD_LTHS[**11:0**]** to ensure that the SDCD circuit functions correctly and produces meaningful results.

The scaling for this register is always the same as the selected FSR sensitivity. See Section 9 for the sensitivity values corresponding to each of the selectable FSRs.

Table 114. SDCD_UTHS_MSB register (address 36h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	SDCD_UTHS[11:8]			
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 115. SDCD_UTHS_MSB register (address 36h) bit description

Field	Description
3 to 0 SDCD_UTHS[11:8]	MSB (nibble) of the signed 12-bit 2's complement upper-threshold value

15.32 SELF_TEST_CONFIG1 register (address 37h)

Table 116. SELF_TEST_CONFIG1 register (address 37h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	ST_IDLE[4:0]				
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 117. SELF_TEST_CONFIG1 register (address 37h) bit description

Field	Description
4 to 0 ST_IDLE	Self-Test Idle phase duration: The value contained in ST_IDLE determines the Self-Test Idle phase duration per Equation 3. $ST_{IDLE} = 312.5\ \mu s + (ST_{IDLE} \times 31.25)\ \mu s$ (3)

15.33 SELF_TEST_CONFIG2 register (address 38h)

Table 118. SELF_TEST_CONFIG2 register (address 38h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	ST_DEC[3:0]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 119. SELF_TEST_CONFIG2 register (address 38h) bit description

Field	Description
3 to 0 ST_DEC	Self-Test measurement phase decimation factor This bit field selects the Self-Test measurement phase decimation factor. The decimation selection ranges from 1 to 4096 as shown in Table 120.

Table 120. Self-Test measurement phase decimation settings

ST_DEC[3]	ST_DEC[2]	ST_DEC[1]	ST_DEC[0]	Decimation selection (Number of samples	Self-Test measurement period (ms)	Self-Test ODR (Hz)
0	0	0	0	1	0.3125	3200
0	0	0	1	2	0.625	1600
0	0	1	0	4	1.25	800
0	0	1	1	8	2.5	400
0	1	0	0	16	5	200
0	1	0	1	32	10	100
0	1	1	0	64	20	50
0	1	1	1	128	40	25
1	0	0	0	256	80	12.5
1	0	0	1	512	160	6.25
1	0	1	0	1024	320	3.125
1	0	1	1	2048	640	1.563
1	1	0	0	4096	1280	0.78125
1	1	0	1	4096	1280	0.78
1	1	1	0	4096	1280	0.781
1	1	1	1	4096	1280	0.781

Notes:

- *During the self-test sequence, the accelerometer measurement period in µs (for each axis and each direction) is given by Equation 4.*

$$ST_{PERIOD}\ \mu s = 2^{ST\_DEC[3:0]} \times [312.5 + (ST\_IDLE[4:0] \times 31.25)\ \mu s] \quad (4)$$

- *The user-selected ODR and power mode settings are ignored during self-test operation. The user-selected settings for ODR and power mode are applied after self-test is disengaged, for example,* ***SENSCONFIG1[...]****ST_AXIS_SEL[1:0] = 00b.*

16 Application information

16.1 System connections

FXLS8967AF connects to a host processor through an I^2C or SPI interface. Figure 19 to Figure 24 show the recommended circuit connections.

16.2 Recommendation for reading data registers

When operating in active mode the sensor stores the acceleration measurement in the associated LSB and MSB Data registers. Assuming Fast Mode Read is not used, it is important to ensure the coherency between MSB and LSB data bytes for a given axis when the host MCU reads those two registers, in order words, they both need to correspond to the same measurement sample.

As mentioned in the registers description, the output data is latched into the OUT_X/Y/Z registers along with the assertion of the SRC_DRDY event flag. Moreover, when the host MCU initiates a data register read transaction on the slave interface (Start condition in I2C mode or SPI_CS transition to low level in SPI mode), the content of all data registers is locked till the transaction is completed. There are actually shadow registers to prevent that data registers are updated when a new sample becomes available.

If the MCU performs single byte read transactions, the coherency between MSB and LSB data bytes cannot be granted as they will be associated to two distinct transactions. Consequently it is highly recommended to use multiple bytes for data reading, in order to at least collect both MSB and LSB data bytes with a unique read transaction. Obviously, the MCU can collect all three axes data simultaneously (6 bytes) with a multiple bytes data reading, and this will also ensure that the XYZ data triplet corresponds to the same timestamp.

Note: *This constraint is mostly valid for asynchronous data reading. It is quite lightened if the host MCU configures the sensor data ready interrupt to perform synchronous (interrupt driven) data reading, as this provides an adequate trigger to read the samples. The synchronous reading scheme is also recommended to avoid unnecessary traffic on the slave interface, such as polling status registers.*

Those considerations applies to normal Data output registers OUT_X/Y/Z, but also to BUFF_X/Y/Z registers and VECM registers.

16.3 Typical application circuits

X7R or X5R ceramic capacitors are recommended for V_{DD} supply decoupling. A 1 µF capacitor in parallel with a 0.1 µF is recommended as a starting point per the NXP EMC test standard. These capacitors should be placed as close to the V_{DD} supply pin as practical. The values of the capacitors can be changed to suit the EMC performance requirements of the application.

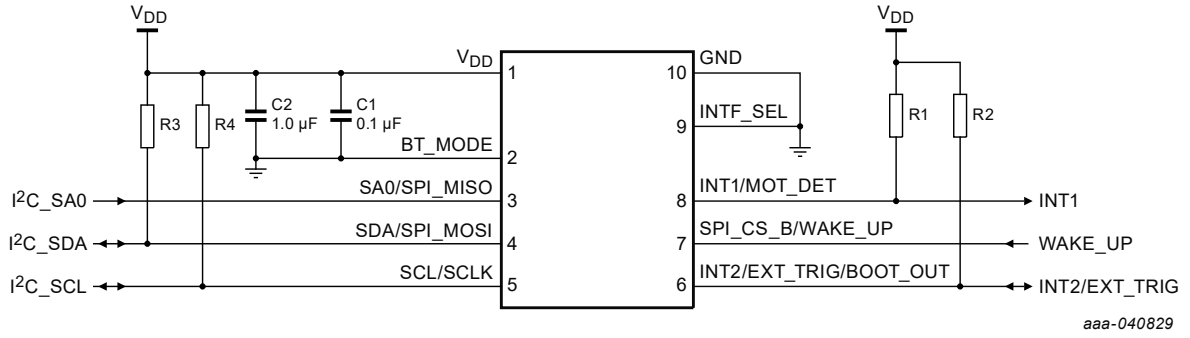


Figure 19. Typical Application Circuit #1 – I^2C mode

Notes:

- *Resistors R1 and R2 are not needed if the interrupt output driver type is configured for push-pull operation (default).*
- *If either the INT1 or INT2 pins are not used in the application, leave them unconnected.*
- *The required pull-up resistor values for R3 and R4 are dependent on several factors including the I^2C clock frequency, bus pull-up voltage, and the total parasitic trace + device capacitances. A suggested starting point is 4.7 kΩ for Standard and Fast modes.*
- *The external trigger function can be used to initiate a single shot measurement of the XYZ acceleration and temperature data. This mode is useful for synchronizing measurements with an external system or for creating user-specific ODRs. The measurement is triggered on the rising edge of the EXT_TRIG signal.*

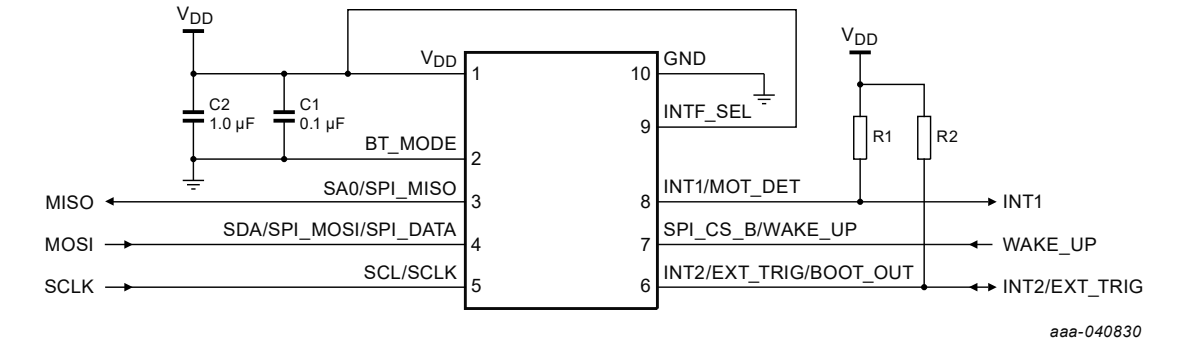


Figure 20. Typical Application Circuit #2 – SPI 4-wire mode

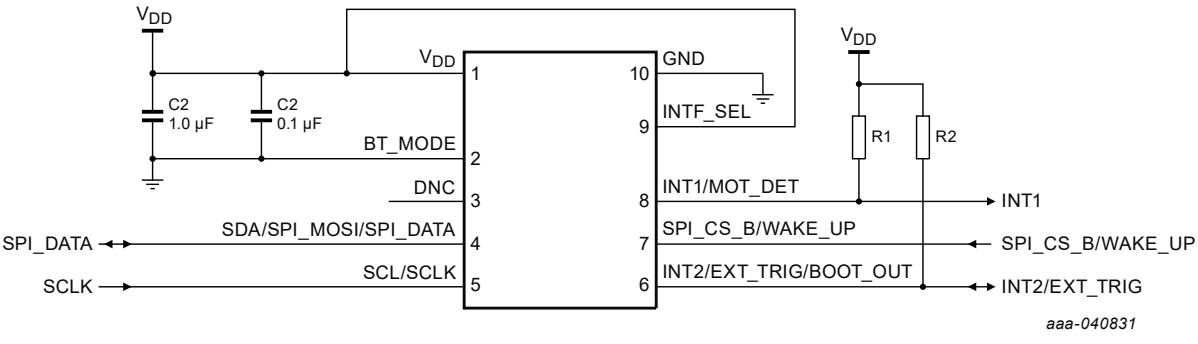


Figure 21. Typical Application Circuit #3 – SPI 3-wire mode (software enabled; SENS_CONFIG1[SPI_M] = 1)

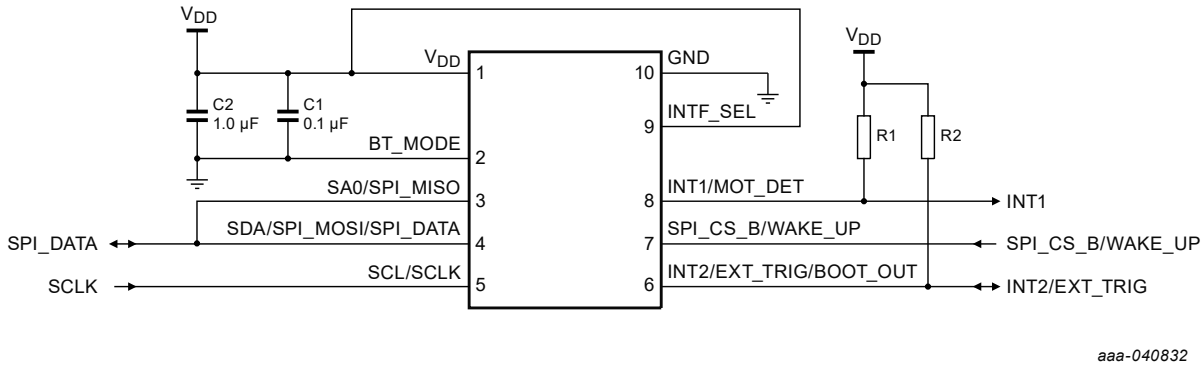


Figure 22. Typical Application Circuit #4 – SPI 3-wire mode (hardwired; SENS_CONFIG1[SPI_M] = X)

Notes:

- *The external trigger function can be used to trigger a single shot measurement of the XYZ acceleration and temperature data. This mode is useful for synchronizing measurements with an external system or for creating user-specific ODRs. The measurement is triggered on the rising edge of the EXT_TRIG signal.*
- *Resistors R1 and R2 are not needed if the interrupt output driver type is configured for push-pull operation (default). A suggested range for open-drain configuration is 10 kΩ to 100 kΩ.*
- *If the INT1 pin, INT2 pin, or both pins are not used in the application, leave the unused pins unconnected.*
- *The SPI_CS_B pin also serves as a signal to wake the device from Hibernate mode.*
- *See Section 13.2 and Section 13.4 for more details on 3-wire SPI mode.*

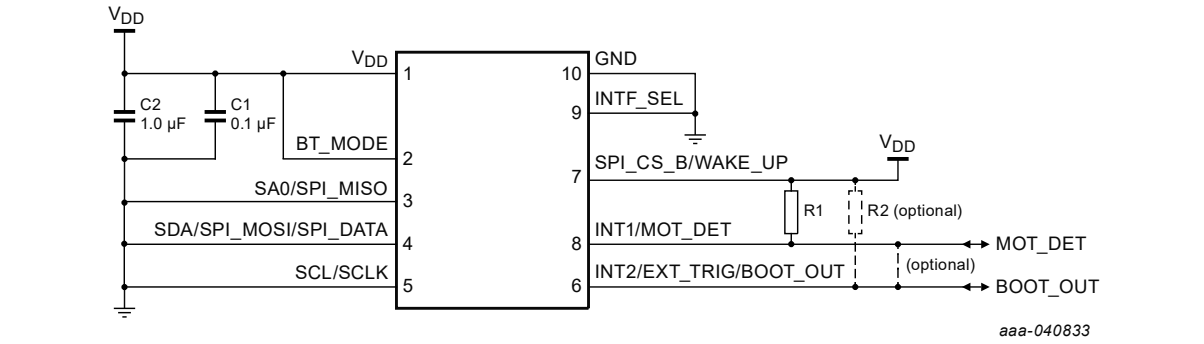


Figure 23. Typical Application Circuit #5 – Motion detection mode (no serial interface)

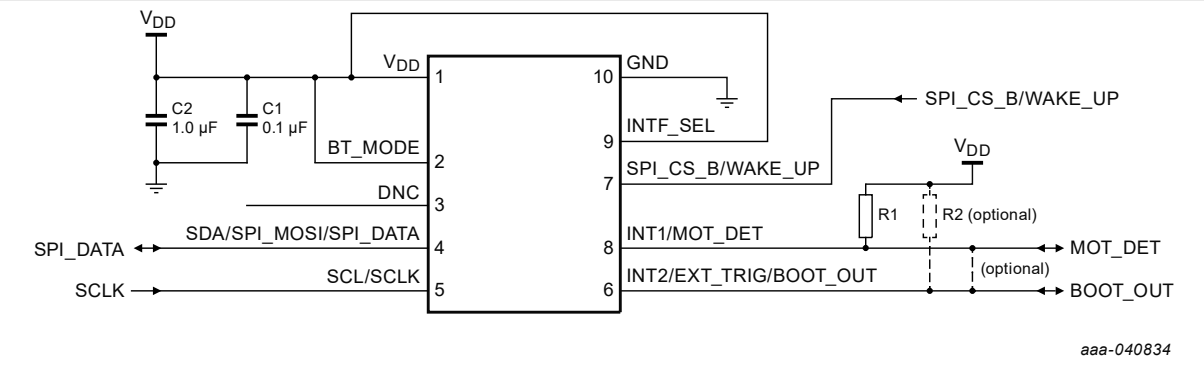


Figure 24. Typical Application Circuit #6 - Motion detection mode (with SPI 3-wire interface, software enabled)

Notes:

- *External resistor R2 is not needed if the BOOT_OUT and MOT_DET pins are tied together (wired AND configuration).*
- *A suggested pull-up resistance range is 1 MΩ to 2.5 MΩ for both R1 and R2 to minimize the power dissipated in the resistor when the line is pulsed low. When BT_MODE is set to V_{DD} (enabling motion detection mode), both the MOT_DET and BOOT_OUT pins become open-drain output driver types. MOT_DET also functions as a CMOS input and is used by the host system to power-manage FXLS8967AF.*
- *When BT_MODE = V_{DD}, the default motion detection parameters are automatically loaded into the device after a POR/BOR event occurs; no configuration via I^2C or SPI is needed if the default parameters are used in the application.*
- *See Section 13.2 and Section 13.4 for more details on 3-wire SPI mode. In motion detection mode with BT_MODE=V_{DD}, use of HPM or FPM mode is not advised. Only the default LPM mode should be used.*

16.4 Power supply considerations

NXP recommends that V_{DD} be sourced from a low noise linear supply regulator (LDO). When using a switch mode supply, the recommended minimum voltage is 1.8 V (nominal), providing headroom for supply noise and ripple rejection. This headroom ensures that the device meets its performance specifications while also preventing a BOR/POR event from occurring when operated on a noisy supply rail.

FXLS8967AF contains a POR generator. This circuit resets the digital logic and restores all register content to the default values shown in Table 20 after applying $V_{DD} \geq 1.71$ V, or after a soft reset command is issued by setting **SENS_CONFIG1[**RST**]** = 1.

Note: *The host system must wait for a nominal time period of $T_{BOOT1/2}$ ms after applying $V_{DD} \geq 1.71$ V, or after issuing a soft reset command, to allow enough time for FXLS8967AF to complete its internal boot sequence and be ready for communication over the I^2C or SPI interfaces.*

When the BT_MODE pin is low, with **INT_EN[**BOOT_DIS**]** = 0, the host system can wait until the active edge of a $T_{PULSE-BOOT1}$ µs pulse is observed on the INTx pin (determined by **INT_PIN_SEL[**BOOT_INT2**]**) indicating completion of the boot sequence. When the BT_MODE pin is logic high, the INT2 pin is configured as an open-drain output (BOOT_OUT) that pulses low for $T_{PULSE-BOOT2}$ ms after the boot sequence completes.

17 Package outline

The FXLS8967AF uses a ten-pin DFN package, case number 98ASA00979D.

17.1 Package description

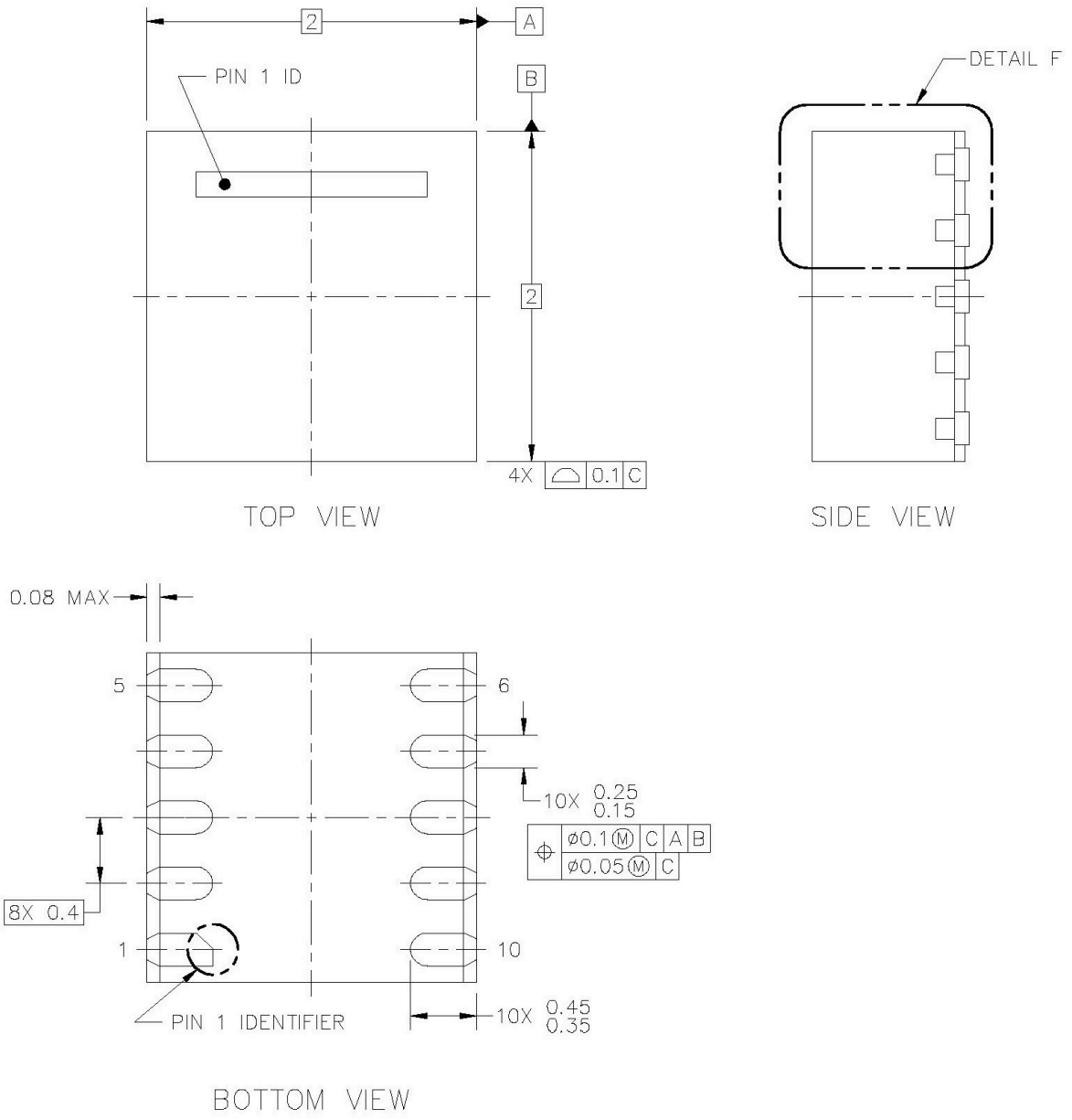
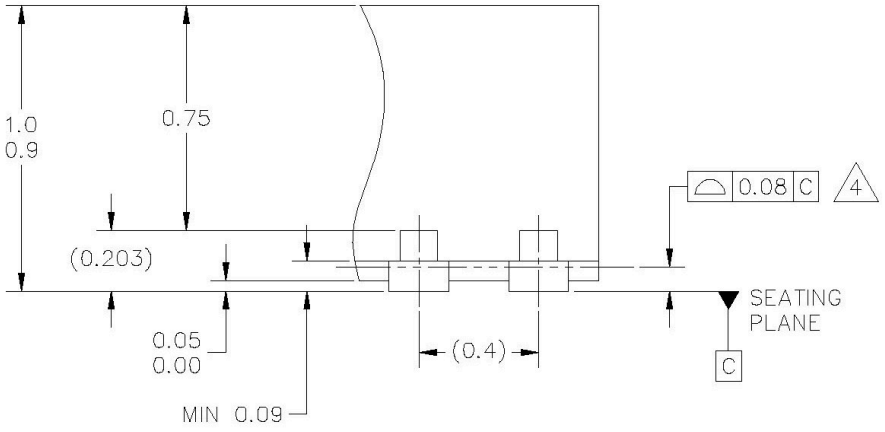


Figure 25. FXLS8967AF package outline



DETAIL F
VIEW ROTATED 90°CW

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TITLE: DFN−COL, PLASTIC DUAL FLAT NON−LEADED PACKAGE, 2 X 2 X 0.95, 0.4 PITCH, 10 TERMINAL	DOCUMENT NO: 98ASA00979D	REV: B
	STANDARD: NON−JEDEC	
	SOT1615−3	18 MAY 2017

Figure 26. FXLS8967AF package outline detail

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS IS A NON–JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS.
5. TOTAL THICKNESS DOES NOT INCLUDE BURR.

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	STANDARD: NON–JEDEC	
	SOT1615–3	18 MAY 2017

Figure 27. FXLS8967AF package outline notes

17.2 Lead dimension detail

The width of lead end as viewed from leaded side of package has minimum dimension of 0.125 mm. The maximum dimension is equal to lead width at the bottom surface of the package as indicated on the drawing.

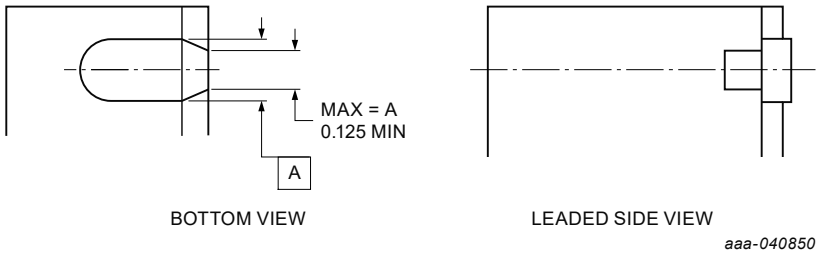

Figure 28. Bottom and leaded view dimensions

17.3 Burr specification

The assembly site specifies burrs to 0.076 mm maximum.

18 Soldering information

18.1 Printed circuit board layout and device mounting

Printed circuit board (PCB) layout and device mounting are critical to the overall performance of the design. The footprint for the surface mount packages must be the correct size as a base for a proper solder connection between the PCB and the package. The correct size of the surface mount package footprint, along with the recommended soldering materials and techniques, optimize assembly and minimize the stress on the package after board mounting.

NXP application note AN1902[1] discusses the DFN package used by the FXLS8967AF.

18.1.1 Overview of soldering considerations

The information provided here is based on experiments executed on QFN devices. They do not represent exact conditions present at a customer site. Therefore, information herein should be used as guidance only, and process and design optimizations are recommended to develop an application-specific solution. It should be noted that with the proper PCB footprint and solder stencil designs, the package self-aligns during the solder reflow process.

18.1.2 Halogen content

This package is Halogen free, exceeding most industry and customer standards. Halogen Free means that no homogeneous material within the assembly package shall contain chlorine (Cl) in excess of 700 ppm or 0.07 % weight/weight or bromine (Br) in excess of 900 ppm or 0.09 % weight/weight.

19 Mounting information

19.1 PCB mounting recommendations

- No additional via, copper layer, solder mask, metal pattern underneath package on the mounted layer of the PCB.
- Do not place any components or vias within 2 mm of the package land area as it may cause additional package stress if placed too close to the package land area.
- Signal traces connected to pads should be as symmetric as possible. To have the same length of exposed trace for all pads, put dummy traces on NC pads .
- Use a standard pick-and-place process and equipment. Do not use a hand soldering process.
- Customers are advised to be cautious about the proximity of screw-down holes to the sensor, and the location of any press fit to the assembled PCB when in an enclosure. It is important that the assembled PCB remain flat after assembly to keep electronic operation of the device optimal.
- The PCB should be rated for the multiple lead-free reflow condition with a maximum 260 °C temperature.
- NXP sensors are compliant with Restrictions on Hazardous Substances (RoHS), having halide-free molding compound (green) and lead-free terminations. These terminations are compatible with tin-lead (Sn-Pb) as well as tin-silver-copper (Sn-Ag-Cu) solder paste soldering processes. Reflow profiles applicable to those processes can be used successfully for soldering the devices.

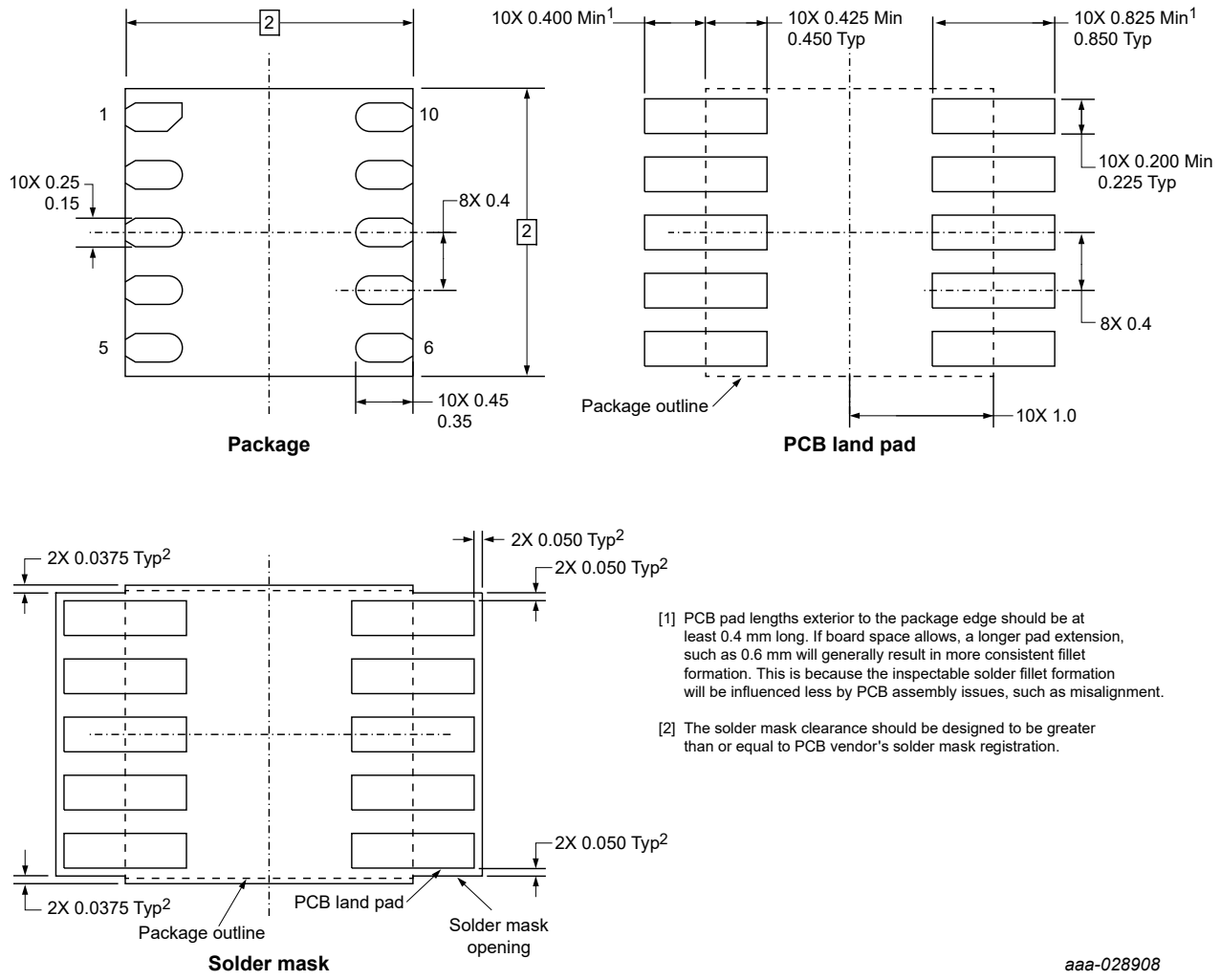

Figure 29. PCB footprint guidelines

20 Glossary

Table 121. Glossary

Term	Description
Cross-axis sensitivity	Cross-axis sensitivity is the ratio of the measured acceleration for an axis to the input acceleration along each axis orthogonal to the measured axis. Cross-axis sensitivity leads to undesirable nonorthogonality of X, Y, and Z axes in the frame of reference of the assembled device when mapping to other frames of reference. Cross-axis sensitivity is expressed as a percentage of the orthogonal input acceleration with six separate cross-axis sensitivity terms known as Sxy, Sxz, Syx, Syz, Szx, and Szy. The cross-axis sensitivity specification represents the maximum of these six terms.

Table 121. Glossary...*continued*

Term	Description
Noise density and RMS-integrated noise	Noise density is defined as the noise per unit of square root bandwidth and is typically expressed in units of mg/√Hz or µg/√Hz for a consumer grade accelerometer. Noise is measured with the device held stationary in a 1*g* field and isolated from environmental noise and mechanical vibration. The RMS noise at a given ODR can be estimated as follows: $N_{rms} = ND * \sqrt{BW}$ For example, in the ±2 *g* FSR, operating in HPM with an ODR of 400 Hz, the estimated RMS noise would be: N_{rms} = 280 µg/√Hz * √(400/2) Hz = 3.96 mg (~ 4 LSB).
Output data rate, decimation factor, and power consumption	The Output Data Rate (ODR) defines the rate at which acceleration data is output from FXLS8967AF. Depending on the operating mode and ODR that is selected, different decimation factors (oversampling ratios) are applied. The decimated output data is supplied at the ODR rate, even though multiple samples of the sensor data may have been used to calculate this average result. In FXLS8967AF lowest power mode, the decimation factor is always 1, leading to the best power performance at the expense of the poorest noise (resolution) performance. In high performance mode, the decimation factor is automatically increased to the maximum possible value for a given ODR, resulting in the best noise (resolution) performance at the expense of the poorest power consumption. In motion detection mode with BT_MODE=V_{DD}, use of HPM or FPM mode is not advised. Only the default LPM mode should be used.
Primary	Device that initiates and drives the communication with secondary devices.
Secondary	Device or devices that responds to communication initiated by primary device.
Self-Test	The integrated self-test function can be used to verify correct transducer and signal chain operation without the need to apply an external acceleration stimulus. When the self-test function is activated for each axis, an electrostatic actuation force is applied to the proof mass, simulating a small change in acceleration. The self-test function of the device is independently exercisable for each axis, along with a selectable displacement direction (polarity). The device need not be static while exercising the self-test function as it is insensitive to any external physical acceleration. During a self-test sequence, 2 parameters are computed for each axis, namely STOC and STOF. STOC is the half difference between Self-Test output for positive direction (ST_POL=0) and Self-Test output for negative direction (ST_POL=1), whereas STOF is the half sum between the same. Refer to AN13193[2] for more details on self-test.
Sensitivity	The accelerometer sensitivity, also known as *scale-factor*, represents the change in acceleration input corresponding to 1 LSB change in output and is typically measured in either mg/LSB or LSB/*g*.
Zero-*g* offset	The accelerometer zero-*g* offset describes the deviation of the sensor output from the ideal 0g value when no motion or gravity is acting on it. With an accelerometer stationary and placed on a level, horizontal surface, the ideal output is 0 *g* for the X and Y axes. Likewise, if the accelerometer is placed on a vertical plane, the ideal output is 0 g for the Z-axis. The deviation of each output from the ideal value is called *zero-g offset*. Offset is, to some extent, a result of stress on the sensor and how well the sensor is leveled when soldered to the board. Therefore, the zero-*g* offset can change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. For applications that require increased precision, any residual post-board mount offset may be removed using the **OFF_X/Y/Z** registers, or alternatively, in the host application software.

21 References

[1] AN1902 — Assembly Guidelines for QFN and DFN Packages, https://www.nxp.com/webapp/Download?colCode=AN1902

[2] AN13193 — Self-test procedure for FXLS896xAF and FXLS897xCF, https://www.nxp.com/docs/en/application-note/AN13193.pdf

[3] UM10204 — I^2C-bus specification and user manual, https://www.nxp.com/webapp/Download?colCode=UM10204

22 Revision history

Table 122. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
FXLS8967AF v.1.5	20220311	Product data sheet	—	FXLS8967AF v.1.4
Modifications:	• Section 2, revised the low noise feature from "280 µg/√Hz" to "230 µg/√Hz".			
FXLS8967AF v.1.4	20220302	Product data sheet	—	FXLS8967AF v.1.3
FXLS8967AF v.1.3	20211022	Preliminary data sheet	—	FXLS8967AF v.1.2
FXLS8967AF v.1.2	20210928	Preliminary data sheet	—	FXLS8967AF v.1.1
FXLS8967AF v.1.1	20210902	Objective data sheet	—	FXLS8967AF v.1
FXLS8967AF v.1	20210427	Objective data sheet	—	—

23 Legal information

23.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Document identifier: FXLS8967AF