

Kinetis KLx6/KL34 to Kinetis KL43/KL33/KL27/KL17 Migration

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1 Introduction

This document describes the details of migrating from Kinetis KLx6/KL34 MCUs to Kinetis KL43/KL33/KL27/KL17 MCUs. Migrating between two devices within the same family can require hardware and/or software changes in some cases. The changes that may be required are described in this document. Note that the “x” in the name KLx6 does not include the lowest family of devices (KL06).

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2 Part Numbering and Mask Set Information

Table 1 lists all of the KLx6 mask sets that are available at the time this document is released.

Table 2 shows the device mask set and part number example for the MCUs that are the source of the migration.

Table 1. KLx6/KL34 mask sets

Revision	Mask set	Part number example
1.0	0N40H	MKL46Z256VLH4

Table 2. KL43/KL33/KL27/KL17 mask sets

Revision	Mask set	Part number example
1.1	1N71K	MKL43Z256VLH4

This document primarily focuses on the migration from the KLx6/KL34 MCUs to the KL17/KL27/KL33/KL43 MCUs within the same Kinetis family. For example, this document is helpful when migrating from the MKL46Z256VLH4 MCU to the MKL43Z256VLH4 MCU. However, this document does not focus on the changes in functionality between the Kinetis L families, for example, between the MKL17Z128VLH4 MCU and the MKL33Z128VLH4 MCU.

3 About This Document

This document describes the migration from the Kinetis KLx6/KL34 MCUs to the Kinetis KL43/KL33/KL27/KL17 MCUs (excluding the KL06 and KL03 families) and is divided into four major sections:

- New modules/features
- Updated modules
- Modules with additional instantiations
- Removed modules

The “new modules/features” section provides a quick overview of modules that are completely new on the KL43/KL33/KL27/KL17 devices. These are the modules that do not have any functional equivalent available in the KLx6/KL34 MCUs. If you plan to use some of these new modules in your application, change the software to use the new module.

The “updated modules” section describes the modules that are updated to use newer versions. The overall functionality is similar; however, changes in software are required. Hardware changes may also be required to use the new features.

The “modules with additional instantiations” sections describe the modules where the modules themselves have not changed, but there are more instantiations of the module included in the MCU.

The “Removed modules” section briefly describes the modules not included on the KL43/KL33/KL27/KL17 MCUs.

Color key	
GREEN	Designates new additions.
YELLOW	Designates changes.
RED	Designates removals.

NOTE

There are slight differences between the KL43/KL33/KL27/KL17 devices with 128/256 KB flash memory and the devices with 32/64 KB flash memory. The devices with 32/64 KB flash memory include, for example, a new CRC module and the new keep-alive feature in the USB module. However, these devices do not include the USB voltage regulator and the DAC module. This also results in pin differences. In this document, the most important differences are mentioned in the form of notes.

4 New Modules and Features

These features are added to the Kinetis KL43/KL33/KL27/KL17 MCUs:

- A lite version of the multi-purpose clock generator module (MCG Lite)
- The voltage reference module (VREFV1)
- The flexible I/O module (FlexIO)
- The low-power UART module (LPUART)

The KL43/KL33/KL27/KL17 MCUs also include a ROM memory with the Kinetis bootloader implemented. These modules and features are not available on the KLx6/KL34 MCUs. The following sections provide an overview of the features of these modules. The applications that use these new modules require software changes (and in some cases also hardware changes) to take advantage of the new functionality.

NOTE

The availability of these modules depends on the specific Kinetis MCU used. See the reference manual for your Kinetis MCU for information on the available features.

4.1 MCG Lite module

This module is not an update to the MCG module available on the KLx6/KL34 MCUs, but it is completely different. However, it shares several configuration registers. The main difference is that the MCG Lite module does not include the FLL and PLL. Therefore, there are no registers related to the FLL and PLL configuration, such as the MCG_C3 through to MCG_C8. The MCG Lite module includes a high-frequency internal reference clock (48 MHz HIRC) and low-frequency internal reference clocks (2 MHz and 8 MHz LIRC).

The maximum available clock source frequency is the 48 MHz HIRC. It supports various trimming capabilities to achieve accuracy of up to 1.5 %. The clock-stabilization latency is greatly reduced using the HIRC (less than 3 μ s versus 1 ms to lock the PLL clock). The HIRC does not support low-power modes. The MCG Lite module enables the HIRC to work with the full-speed USB in the so-called USB clock recovery mode (available only in the full-speed USB device mode). The USB module monitors the HIRC clock and adjusts the fine trim according to its default values. Using this implementation, it is possible to achieve clock accuracy higher than 1.5 %.

It is possible to configure the LIRC (2 MHz and 8 MHz) as the clock source for the VLPR mode and make it work in all low-power modes, except for the low-leakage modes (such as MCGIRCLK). The MCG Lite is turned off in all low-leakage modes (LLS, VLLSx). Note that there is no support to switch between the 2-MHz and 8-MHz LIRC modes directly, because they share the same logic circuit. Switch to another clock mode (HIRC or EXT mode) and then switch to the appropriate LIRC mode (this is not enabled in the VLPR mode).

Select from four different clock modes (see [Figure 1](#)) with these clock sources:

- HIRC mode—high-frequency (48 MHz) internal reference clock named HIRC48 (with a USB recovery feature that enables drastic reduction of the jitter).
- LIRC 8-MHz mode (default after reset)—low-frequency 8-MHz internal reference clock.
- LIRC 2-MHz mode—low-frequency 2-MHz internal reference clock.
- EXT mode—external clock source (available also on the KLx6/KL34 MCUs):
 - Low-frequency mode (1–32.768 kHz).
 - High-frequency mode 1 (1–8 MHz), the KLx6/KL34 MCUs use 3–8 MHz.
 - High-frequency mode 2 (8–32 MHz for the crystal, and up to 48 MHz for the external square-wave clock).

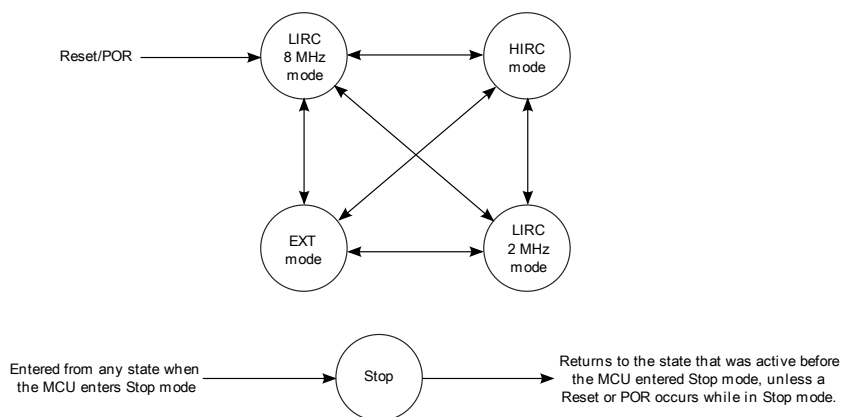


Figure 1. MCG Lite clock mode switching diagram

Some of the registers implemented in the MCG Lite share the same fields with the MCG module. The following figures represent the selected registers with colored fields (the color representation is explained in [Section 3, “About This Document”](#)). All features related to the FLL and PLL are removed (red color).

The MCG_C1 register is shown in Figure 2. The clock source selection field is basically the same as in the MCG module. A slight difference can be found in the IRCLKEN bit, when compared to the MCG (on KLx6/KL34). This field controls the enablement of the low-frequency (2–8 MHz) internal reference clock (LIRC). The same field in the MCG module represents the enablement of the internal reference clock to be used as MCGIRCLK. The IREFSTEN field represents the same functionality. It enables the internal reference clock to be used in the stop mode.

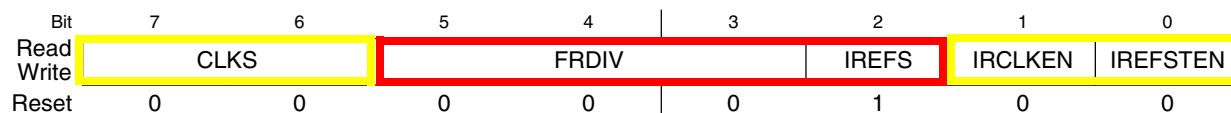


Figure 2. MCG_C1 register differences

The control and status registers MCG_C2, MCG_S, and MCG_SC share the same fields with the same functionality as the MCG (on KLx6/KL34), except for the fields related to the FLL and PLL, which are removed (see figures below).

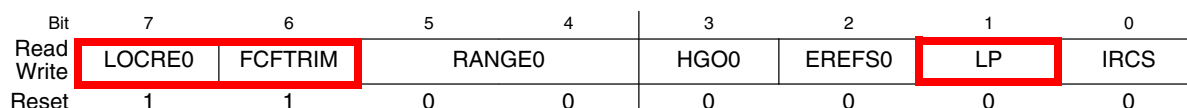


Figure 3. MCG_C2 register differences

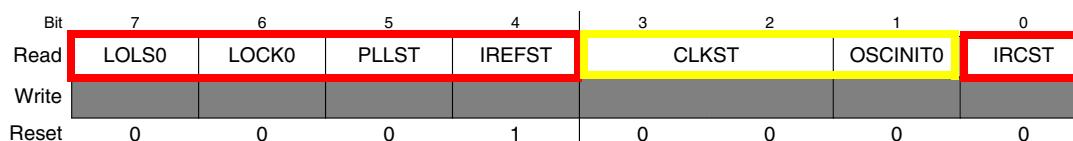


Figure 4. MCG_S register differences

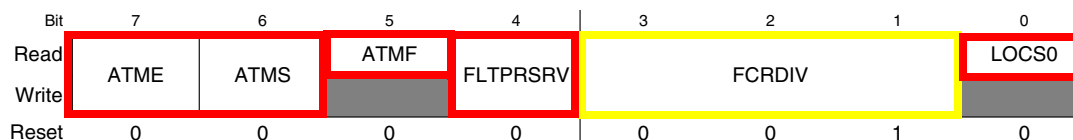


Figure 5. MCG_SC register differences

The MCG miscellaneous control register represents a completely new register implemented in the MCG Lite module. It contains two fields. The HIRCEN field enables the HIRC. The LIRC_DIV2 represents the second LIRC divider, which may be applied only to divide down the clock on the MCGIRCLK output.

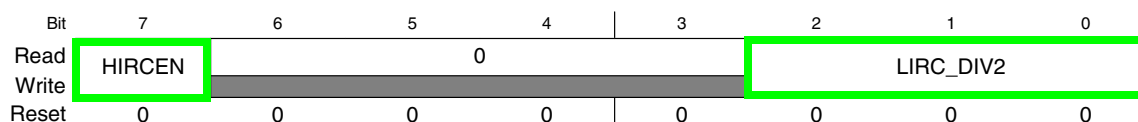


Figure 6. New register MCG_MC

4.1.1 Software impact

Only the EXT mode is not impacted when moving software from the KLx6/KL34 MCUs to the KL43/KL33/KL27/KL17 MCUs. The remaining clock modes are completely different and require a software overhead. If you use the FLL or PLL on the KLx6/KL34 MCUs, move to the appropriate clock mode of the MCG Lite (see the following table).

Table 3. MCG to MCG Lite clock mode equivalents

KLx6/KL34 MCG mode	KLx3 MCG Lite mode equivalent
FEI	HIRC / 8-MHz LIRC / 2-MHz LIRC
FBI	HIRC / 8-MHz LIRC / 2-MHz LIRC
BLPI	LIRC (divided down to 4 MHz or lower)
FEE	EXT mode
FBE	EXT mode
BLPE	EXT mode (lower than 4 MHz)
PBE	EXT mode
PEE	EXT mode

4.1.2 Hardware impact

There is no hardware impact.

4.2 VREFV1 module

The KL43/KL33/KL27/KL17 MCUs also include the voltage reference, which may be used internally for the ADC, CMP, or DAC modules, and by the external devices. The voltage reference level is set to 1.2 V (via 0.5 mV programmable steps) using a trim register (see the device data sheet for the minimum and maximum voltage rating specifications). The maximum output current for the high-power mode is 1 mA. Build the hardware carefully and remember that the voltage reference output pin (VREF_OUT) is shared with the VREFH pin. When the voltage reference module is enabled, connect a 100 nF capacitor to the VREFH (VREF_OUT) pin.

4.2.1 Software impact

There is no software impact when using the VREFV1 module.

4.2.2 Hardware impact

The VREFH pin is shared with the VREF_OUT pin. When enabling the VREF module, connect a 100 nF capacitor to this pin. There is a potential hardware conflict when the VREFH uses an external reference source and the VREF is enabled.

NOTE

Be careful with the VREF_OUT pin assignment and read the respective device reference manual and datasheet carefully. There are package differences as well as flash size differences between the particular devices. Generally, the VREF_OUT pin is shared with the VREFH pin (on all devices with packages containing more than 36 pins). However, there are some limitations:

- On the KL43/KL33/KL27/KL17 MCUs with 128/256 KB flash and 36-pin packages (or lower), the VREF module is not available and it is prohibited to enable it.
- On the KL43/KL33/KL27/KL17 MCUs with 32/64 KB flash and 36-pin packages (or lower), the VREF_OUT pin is shared with the PTE30 pin.

4.3 FlexIO module

The FlexIO module is completely new for the Kinetis L portfolio and it is a complex and highly configurable module. Use it to perform emulations of serial/parallel communication protocols, such as UART, I²C, I²S, and SPI (using one module). However, the FlexIO module is not limited to communication. It can be used as a PWM signal generator, an LCD RGB, or as a pure programmable digital logic block (and many other options).

The FlexIO includes four main features:

- Four 32-bit double-buffered shift registers with transmit, receive, and data match modes. Each shift register also supports a read/write capability with bit-byte swap, byte swap, and bit swap.
- Four 8- or 16-bit (depends on the mode selection) timers with a highly flexible configuration.
- Eight I/O pins (for shifter/timer input/output with polarity selection).
- Sixteen triggers (external or internal, such as a shifter, a timer, or a pin, with polarity selection).

The FlexIO module supports the ability to work in the Debug mode and the asynchronous operation during the Stop mode (except for the low-leakage modes). The IRQ, DMA, or pure polling operations are supported.

4.3.1 Software impact

There is no software impact when using the FlexIO module.

4.3.2 Hardware impact

There is no hardware impact when using the FlexIO module.

4.4 LPUART module

The LPUART module that is available on the KL43/KL33/KL27/KL17 MCUs (LPUART0, LPUART1) is a new module. It provides features similar to the UART0 module available on the KLx6/KL34 MCUs. The main difference is in the register access. The LPUART module (KL43/KL33/KL27/KL17) uses 32-bit

registers and the UART0 module (KLx6/KL34) uses 8-bit registers. There are also some additional new features on the LPUART:

- Match feature expansion:
 - Match configuration (MATCFG).
 - Address match wakeup (default on the UART0 on the KLx6/KL34 MCUs).
 - Idle match wakeup.
 - Match on and match off.
 - RWU enablement on the data match and match on/off for the transmitter CTS input.
 - IRQ generation on the received data match event (MAXIE, MAXF).
 - Match address extension from the 8-bit length to the 10-bit length.
- Configuration of the IDLE flag generation by the number of idle characters received (IDLECFG).
- Status flags for 9-bit and 10-bit data transfers (NOISY, PARITYE, FRETSC, RXEMPT, IDLINE).

Figure 7 shows all differences between the UART0 module available on the KLx6/KL34 MCUs and the LPUARTx module available on the KL43/KL33/KL27/KL17 MCUs. The blue text in the figure represents the 8-bit fields in the 32-bit LPUART module registers that are identical to the UART0 registers. The only exception is the LPUARTx_BDH register. It includes an 8-bit field with content similar to the UART0_C5, but with a new feature related to the match configuration. The green text in the figure represents the new features available on the LPUART.

NOTE

Even the LPUART registers that include some identical features are located at completely different address offsets in the memory (see Figure 7).

UART0 KLx6/KL34		LPUARTx KLx3	
UARTx_BDH	0x400y_z000	LPUARTx_BDH	UARTx_BDL
UARTx_BDL	0x400y_z001		UARTx_BDH
UARTx_C1	0x400y_z002		MATCHCFG UARTx_C5
UARTx_C2	0x400y_z003		UARTx_C4
UARTx_S1	0x400y_z004	LPUARTx_STAT	
UARTx_S2	0x400y_z005		MA2F MA1F
UARTx_C3	0x400y_z006		UARTx_S1
UARTx_D	0x400y_z007		UARTx_S2
UARTx_MA1	0x400y_z008	LPUARTx_CTRL	UARTx_C1
UARTx_MA1	0x400y_z009		IDLECFG MA1IE MA2IE
UARTx_C4	0x400y_z00A		UARTx_C2
UARTx_C5	0x400y_z00B		UARTx_C3
	0x400y_z00C	LPUARTx_DATA	UARTx_D
			8. and 9. bit of data + special status flags
	0x400y_z010	LPUARTx_MATCH	UARTx_MA1
			UARTx_MA2
			8. and 9. bit for MA1

Figure 7. Primary differences between UART0 (KLx6/KL34) and LPUART (KL43/KL33/KL27/KL17)

4.4.1 Software impact

Consider all the previously discussed differences when moving from the KLx6/KL34 MCUs to the KL43/KL33/KL27/KL17 MCUs. If the header file uses the new 8-bit assigned register offsets and the new register fields are not used, then it is software compatible.

4.4.2 Hardware impact

There is no hardware impact when using the FlexIO module.

4.5 CRC module

The KL43/KL33/KL27/KL17 MCUs with 32/64 KB flash also include a cyclic redundancy check (CRC) module that enables generating a 16-bit/32-bit CRC for error detection.

4.5.1 Software impact

There is no software impact.

4.5.2 Hardware impact

There is no hardware impact.

NOTE

The CRC module is not available on the KL43/KL33KL/27/KL17 MCUs with 128/256 KB flash.

4.6 Boot option and ROM with Kinetis bootloader

The 16 KB ROM memory with a built-in Kinetis bootloader (Kibble) is another new feature available on the KL43/KL33/KL27/KL17 MCUs. There is a hardware logic at the boot time that starts the execution from the flash memory (at address 0x0000 0000) or starts the execution of the Kibble from ROM (at address 0x1C00 0000). Select the boot option via the flash non-volatile option byte in the flash configuration field located in the program flash memory (at address 0x40D), and read it by the flash option register FTFA_FOPT located in the peripheral memory region (at address 0x4002 0003). [Figure 8](#) shows the new boot features implemented in the KL43/KL33/KL27/KL17 MCUs. In general, there are two options to boot from the ROM or the flash memory:

- Using an external pin configuration via the BOOTCFG0 pin, which is shared with the NMI pin. This option is selected when the NMI function is enabled and the BOOTPIN_OPT is 0:
 - When the BOOTCFG0 is low, the boot starts from the ROM location.
 - When the BOOTCFG0 is high, the boot starts from the flash memory location.
- Using an internal configuration via the BOOTSRC_SEL field in the flash option field. This option is selected when the external pin configuration is disabled, which means BOOTPIN_OPT = 1. In that case, the BOOTSRC_SEL field selects the boot source.

In the default mode, the boot option is set to ROM because all bits in the FOPT field are set to logical 1. The previously mentioned options are available and take place after each power-on reset (POR). There is another boot option that can force booting from ROM with a specified configuration (external pin or boot source selection, or both) after any system reset (except for POR). This option is available via the reset control module and is explained below.

The built-in bootloader (Kibble) simplifies the programming of the flash memory. All available flash memory programming APIs can run from ROM and write directly into the flash memory. Kibble supports multiple interfaces, such as USB, UART, I²C, or SPI (depending on the Kinetis family implementation).

The additional difference between the two MCUs is the low-power boot option (the yellow area in [Figure 8](#)). The KL43/KL33/KL27/KL17 MCUs support booting into the low-power run mode (VLPR), which can rapidly decrease the current peaks after a reset appears (for example, a wakeup event from the low-leakage modes).

NOTE

Writing into the internal flash memory is not supported when the MCU runs in the VLPR mode. For example, when the device is configured to boot to the VLPR mode and you want to write into the flash memory, switch to the normal Run mode before writing into the flash memory.

Bit Num	Field	Value	Definition
7-6	BOOTSRC_SEL		Boot Source Selection: these bits select the boot sources if boot pin option bit BOOTPIN_OPT = 1
		00	Boot from Flash
		01	Reserved
		10	Boot from ROM
		11	Boot from ROM
5	FAST_INIT		Selects initialization speed on POR, VLLSx, and any system reset.
		0	Slower initialization: The flash initialization will be slower with the benefit of reduced average current during this time. The duration of the recovery will be controlled by the clock divider selection determined by the LPBOOT setting.
		1	Fast Initialization: The flash has faster recoveries at the expense of higher current during these times.
3	RESET_PIN_CFG		Enables/disables control for the RESET pin.
		0	RESET pin is disabled following a POR and cannot be enabled as reset function. When this option is selected, there could be a short period of contention during a POR ramp where the device drives the pinout low prior to establishing the setting of this option and releasing the reset function on the pin. This bit is preserved through system resets and low-power modes. When RESET pin function is disabled, it cannot be used as a source for low-power mode wake-up. NOTE: When the reset pin has been disabled and security has been enabled by means of the FSEC register, a mass erase can be performed only by setting both the Mass Erase and System Reset Request fields in the MDM-AP register.
		1	RESET_b pin is dedicated. The port is configured with pullup enabled, open drain, passive filter enabled.
2	NMI_DIS		Enables/disables control for the NMI function.
		0	NMI interrupts are always blocked. The associated pin continues to default to NMI pin controls with internal pullup enabled. When NMI pin function is disabled, it cannot be used as a source for low-power mode wake-up.
		1	NMI_b pin/interrupts reset default to enabled.
1	BOOTPIN_OPT		External pin selects boot options
		0	Force Boot from ROM if BOOTCFG0 asserted, where BOOTCFG0 is the boot config function which is muxed with NMI pin. RESET pin must be enabled when this option is selected.
		1	Boot source configured by FOPT[7:6] (BOOTSRC_SEL) bits
4,0	LPBOOT		Controls the reset value of OUTDIV1 value in SIM_CLKDIV1 register, and the state of the RUNM register in SMC_PMCTRL. Larger divide value selections produce lower average power consumption during POR, VLLSx recoveries and reset sequencing and after reset exit. The recovery times are also extended if the FAST_INIT option is not selected. ¹
		00	Core and system clock divider (OUTDIV1) is 0x7 (divide by 8). Device is configured for VLPR mode on exit from reset.
		01	Core and system clock divider (OUTDIV1) is 0x3 (divide by 4). Device is configured for VLPR mode on exit from reset.
		10	Core and system clock divider (OUTDIV1) is 0x1 (divide by 2). Device is configured for RUN mode on exit from reset.
		11	Core and system clock divider (OUTDIV1) is 0x0 (divide by 1). Device is configured for RUN mode on exit from reset.

Figure 8. New and changed boot options available on KL43/KL33/KL27/KL17 MCUs (green area)—in flash memory non-volatile option byte

4.6.1 Software impact

There is no software impact when using the boot option and ROM with the Kinetis bootloader.

NOTE

The default boot source on the KL43/KL33/KL27/KL17 MCUs is ROM. Expect some latency due to ROM code execution when compared to the KLx6/KL34 MCUs where the flash memory is the default boot source. To avoid the ROM boot latency, change the BOOTSRCSEL in the flash configuration field to 0x0 (boot from flash) in software.

4.6.2 Hardware impact

There is no hardware impact when using the boot option and ROM with the Kinetis bootloader.

NOTE

Do not connect a capacitor to the PTA4 (NMI) when using the BOOTCFG pin as a ROM/flash boot selector with the KL43/KL33/KL27/KL17 MCUs (as usually done by a button with the RC filter for the NMI functionality). The charging of a capacitor causes the program to enter the ROM boot. Hence, the ROM code latency occurs after a reset.

5 Modules/Features Updates and Differentiations

5.1 NVIC interrupt vector differences

There are some changes in the NVIC related to the interrupt vectors. All expected differences are highlighted in this table:

Table 4. NVIC interrupt vectors update

Address	Vector	IRQ	KLx6/KL34		KL43/KL33/KL27/KL17	
—	—	—	Source module	Source description	Source module	Source description
0x0000_0070	28	12	UART0	Status and error	LPUART0	LPUART0 status and error
0x0000_0074	29	13	UART1	Status and error	LPUART1	LPUART1 status and error
0x0000_0078	30	14	UART2	Status and error	UART2 or FLEXIO	UART2 status and error or all integrated FlexIO flags
0x0000_00A0	40	24	USB0	USB0 interrupt (OTG)	USB	USB interrupt (FS device)
0x0000_00A2	42	26	TSI0	TSI interrupt	—	Reserved
0x0000_00A3	43	27	MCG	Loss of external clock + loss of lock	—	Reserved

5.1.1 Software impact

The appropriate callback function is called in the interrupt service routine on the basis of interrupt flag checking in the case of shared UART2 and FlexIO vectors. Recognize the UART2 interrupt (KLx6/KL34) in the interrupt service routine, otherwise the program flow is not going to be correct. The service routines related to the interrupt vectors that are not defined (especially TSI and MCG) are not used. Additional software overhead is caused by the use of different names.

5.1.2 Hardware impact

There is no hardware impact considering the NVIC interrupt vector differences.

5.2 AWIC wakeup source differences

There are some differences in the AWIC wakeup sources that are used to exit the stop modes (except for the low-leakage stop modes). The AWIC wakeup sources are related to peripherals similar to those mentioned in [Section 5.1, “NVIC interrupt vector differences”](#) and they are highlighted in this table:

Table 5. AWIC wakeup sources update

KLx6/KL34		KLx3	
Wake-up source	Description	Wake-up source	Description
UART0	Any interrupt-provided clocks remain enabled	LPUART0, LPUART1	Any enabled interrupt can be the source as long as the module remains clocked.
UART1, UART2	Active edge on RXD	UART2	Active edge on RXD
TSI	Any interrupt	—	—
—	—	FlexIO	Any enabled interrupt can be the source as long as the module remains clocked.

5.2.1 Software impact

Consider the software overhead related to the TSI module when using the KL43/KL33/KL27/KL17 MCUs.

5.2.2 Hardware impact

A potential hardware conflict exists when using the TSI module.

5.3 LLWU wakeup source differences

There is only one difference in the LLWU wakeup source on the KL43/KL33/KL27/KL17 MCUs. The internal peripheral flags LLWU_M4IF do not have any effect on the KL43/KL33/KL27/KL17 MCUs because the TSI module is not implemented.

5.3.1 Software impact

Consider the software overhead related to the TSI module when using the KL43/KL33/KL27/KL17 MCUs.

5.3.2 Hardware impact

A potential hardware conflict exists when using the TSI module.

5.4 System integration module (SIM)

The KL43/KL33/KL27/KL17 SIM module includes the changes described in this section. Because the SIM module interacts with most of the peripheral modules (optional setting for some peripherals, clock-gated control, and so on) it also includes new features related to the new modules.

The specific feature available on the KL43/KL33/KL27/KL17 MCUs is the ability to configure the PTE0 and PTE20 pins as the 32 K oscillator clock output. This feature is available via the system option register SIM_SOPT1 (see the following figure).

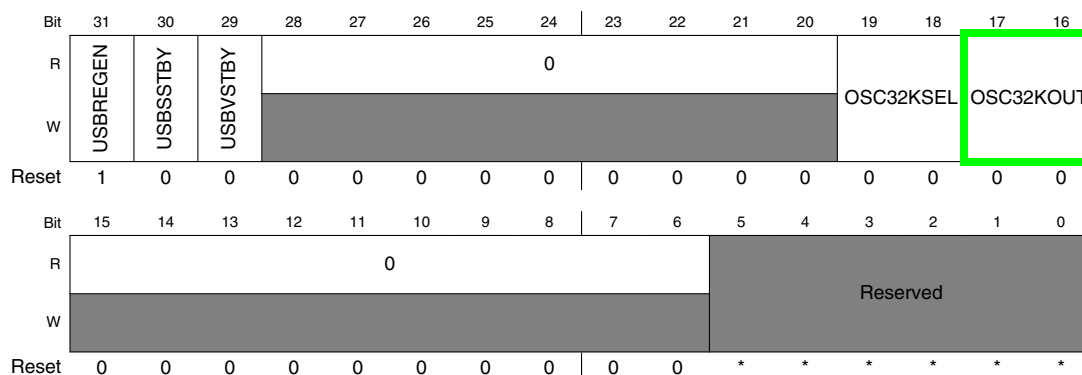


Figure 9. SIM_SOPT1 register new field

The system option SIM_SOPT2 includes new features related to the LPUART1 and FlexIO modules. These are completely new features on the KL43/KL33/KL27/KL17 MCUs. Both modules keep the functionality in the stop modes (except for the low-leakage stop modes). Therefore, they require the ability to be clocked asynchronously, as in the case of LPUART0 or TPM (these two modules are available on the KLx6/KL34 MCUs). The selection of the clock source for both modules is available in the SIM_SOPT2 register (see [Figure 10](#)). The modules use the new field names (LPUART1SRC and FLEXIOSRC) and the LPUART0SRC is renamed (LPUART0SRC instead of UART0SRC).

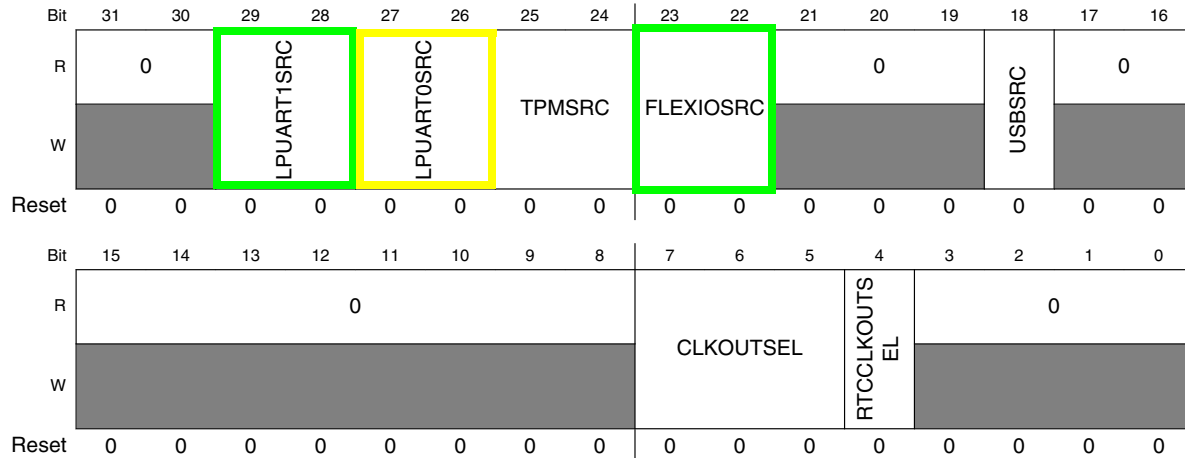


Figure 10. SIM_SOPT2 register new fields

A similar difference is in the system option register 5 (SIM_SOPT5). All register fields are renamed in accordance to the low-power feature (LP).

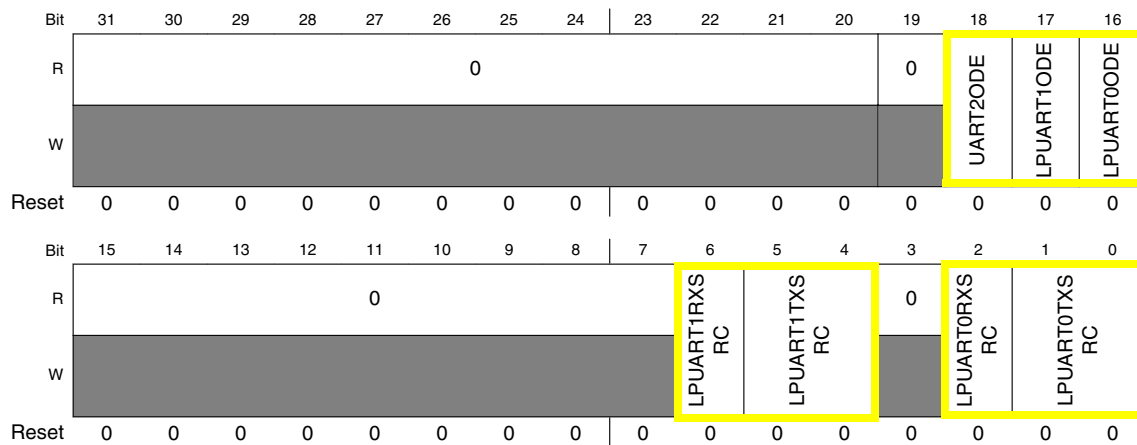


Figure 11. 11 SIM_SOPT5 register new field

The new modules available on the KL43/KL33/KL27/KL17 MCUs require clock-gate control. Therefore, the modules are defined in the system clock-gate control register in the SIM module. The clock-gate control for the VREF module is defined in the SIM_SCGC4 register (see Figure 11). The USB clock-gate control uses a new name of the bit field in the SIM_SCGC4 register. The USBOTG (USB on-the-go) bit used on the KLx6/KL34 MCUs is renamed to USBFS on the KL43/KL33/KL27/KL17 MCUs that support only the device class. The new modules' (FLEXIO, LPUART0, and LPUART1) clock-gate control is defined in the SIM_SCGC5 register.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	1				0						0	VREF	CMPO	USBFS		0
W									SPI1	SPI0						
Reset	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		0	UART2	0	0	0	0				1		0		
W									I2C1	I2C0						
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Figure 12. SIM_SCGC4 register—new and updated fields

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	FLEXIO	0										LPUART1	LPUART0	SLCD		0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		PORTE	PORTD	PORTC	PORTB	PORTA		1	0	0		0		1	LPTMR
W																
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0

Figure 13. SIM_SCGC5 register—new fields

The KL43/KL33/KL27/KL17 MCUs include changes in the COP watchdog. The COP is updated by three new fields in the SIM_COPC register (see [Figure 14](#)). The main difference is the selection of the clock source for the COP watchdog. Except for the LPO and BUSCLK (available also on the KL43/KL33/KL27/KL17/KL34 MCUs), you may choose from two additional clock sources (MCGIRCLK and OSCERCLK).

There is a small difference in the timeout selection. There are more options for the number of cycles to be chosen by each clock source. The short timeout option can be chosen from 25, 28, and 210 cycles (on the KLx6/KL34 MCUs, this option is valid only if the clock source is LPO). The long timeout option can be chosen from 213, 216, and 218 cycles (on the KLx6/KL34 MCUs, this option is valid only if the clock source is BUSCLK). The new feature on the KL43/KL33/KL27/KL17 MCUs is the functionality to work in the Debug and Stop modes.

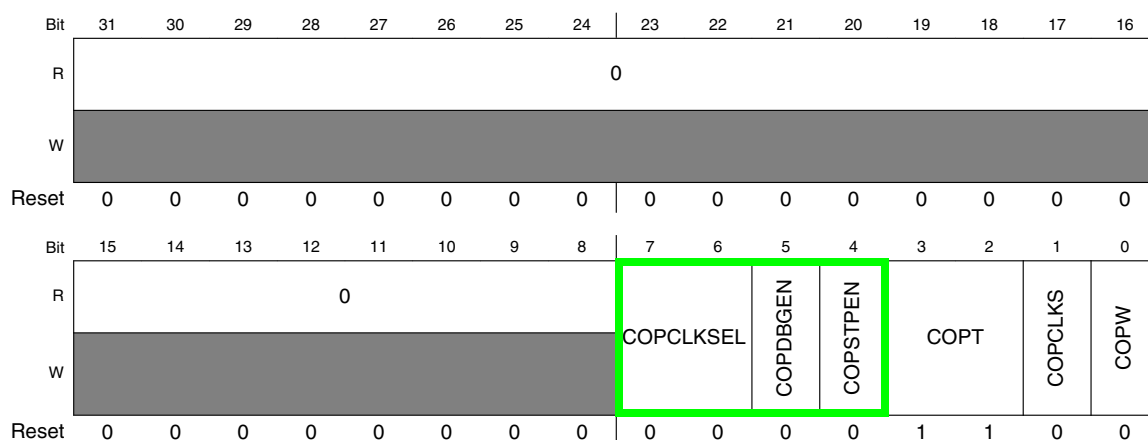


Figure 14. COP control register SIM_COPC register update

5.4.1 Software impact

When using the SIM, there is a software overhead in different bit-field names that are shared by the two MCUs.

5.4.2 Hardware impact

There is no hardware impact when using the SIM.

5.5 RCM update

The reset control module (RCM) on the KL43/KL33/KL27/KL17 MCUs is updated with these two new features:

- Boot source force and boot source identification.
- Sticky system reset status.

Besides the boot option provided by the flash option FOPT, there is also the possibility to force booting by setting the appropriate bits in the force mode register RCM_FM (using the force ROM boot configuration field FORCEROM, see the following figure). The RCM_FM with the FORCEROM option can force booting from the ROM with the specified setting in the boot source mode register RCM_MR.

The force-boot option takes place after all subsequent system resets.



Figure 15. New RCM_FM force mode register

Identify the last boot source by the boot ROM configuration status in the RCM_MR register, as shown in [Figure 16](#) (if not cleared earlier by software). The four boot sources are:

- Boot from flash memory.
- Boot from ROM, caused by:

- External BOOTCFG0 pin.
- Boot source selection BOOTSRC_SEL.
- Both the BOOTCFG0 and BOOTSRC_SEL.

The RCM_MR is also affected by the previously-mentioned force ROM boot setting. This is a read-once—write-once register.

Bit	7	6	5	4	3	2	1	0
Read	0				0	BOOTROM		0
Write					0	w1c		
Reset	0	0	0	0	0	*	*	0

Figure 16. New mode register RCM_MR

The sticky reset status flags represent a new feature implemented on the KL43/KL33/KL27/KL17 MCUs. The sticky reset status flags are available via the sticky system status registers RCM_SSRS0/1. Use these status registers to identify all reset sources generated since the last POR, LVD, or VLLS wakeup (if not cleared previously by software). These status flags are implemented in the same fashion as the system reset status flags in the RCM_SRS0/1 registers with an 8-Byte offset.

Bit	7	6	5	4	3	2	1	0
Read	SPOR	SPIN	SWDOG	0		0	SLVD	SWAKEUP
Write	w1c	w1c	w1c				w1c	w1c
Reset	1	0	0	0	0	0	1	0

Figure 17. New sticky system reset status register 0 (RCM_SSRS0)

Bit	7	6	5	4	3	2	1	0
Read	0	0	SSACKERR	0	SMDM_AP	SSW	SLOCKUP	0
Write			w1c		w1c	w1c	w1c	
Reset	0	0	0	0	0	0	0	0

Figure 18. New sticky system reset status register 1 (RCM_SSRS1)

5.5.1 Software impact

There is no software impact when using the updated reset control module.

5.5.2 Hardware impact

There is no hardware impact when using the updated reset control module.

5.6 DMA MUX differences

The following table highlights the main differences in the DMA request sources between the KL43/KL33/KL27/KL17 and KL46/34 MCUs. The update is in the LPUART1 sources 4 and 5. The DMA source also supports asynchronous requests when in the Stop mode (VLPS and normal STOP). The new FlexIO module has four new sources (10–13). This source also supports asynchronous DMA requests. The last difference is in the TSI source, which is not included on the KL43/KL33/KL27/KL17 MCUs.

Table 6. AWIC wake-up sources update

Source number	KLx6/KL34			KLx3		
	DMA request sources	Source description	Async DMA capable	DMA request sources	Source description	Async DMA capable
—						
2	UART0	Receive	Yes	LPUART0	Receive	Yes
3	UART0	Transmit	Yes	LPUART0	Transmit	Yes
4	UART1	Receive	No	LPUART1	Receive	Yes
5	UART1	Transmit	No	LPUART1	Transmit	Yes
10	Reserved	—	—	Flex_IO	FlexIO_Ch0	Yes
11	Reserved	—	—	Flex_IO	FlexIO_Ch1	Yes
12	Reserved	—	—	Flex_IO	FlexIO_Ch2	Yes
13	Reserved	—	—	Flex_IO	FlexIO_Ch3	Yes
57	TSI	—	Yes	—	—	—

5.6.1 Software impact

The DMA request based on the TSI module does not have an effect. Remove the software related to this feature.

5.6.2 Hardware impact

The TSI module is not available on the KL43/KL33/KL27/KL17 MCUs.

5.7 DAC module update

The new feature in the DAC module of the KL43/KL33/KL27/KL17 MCUs is the FIFO buffer work mode, which is selected via the DAC control register DAC0_C1 (field DACBFMD). In this mode, the DAC buffer (data registers DAC0_DATx) is organized as a FIFO. Any valid write to the DAC data register (the data access restriction is described in the reference manual) increases the write pointer and puts the data into the FIFO format.

NOTE

The DAC module is not available on the KL43/KL33/KL27/KL17 MCUs with 32/64 KB flash memory.

5.7.1 Software impact

There is no software impact when using the updated DAC module.

5.7.2 Hardware impact

There is no hardware impact when using the updated DAC module.

5.8 UART module updates and differences

The UART2 module available on the KL43/KL33/KL27/KL17 MCUs includes the basic features of the UART0/UART1/UART2 modules available on the KLx6/KL34 MCUs. The UART2 module on the KL43/KL33/KL27/KL17 MCUs includes these features:

- Address match wake-up feature (this feature is also available on the UART0, but not on the UART1/UART2 of the KLx6/KL34 MCUs).
- ISO 7816 protocol support.

This section describes the differences between the UART2 module on the KL43/KL33/KL27/KL17 MCUs and the UART0/UART1/UART2 modules on the KLx6/KL34 MCUs. The UART2 module does not support the LIN break detection and data characters with two stop bits. These features are also removed from the registers, especially from the **baud rate register high register** UARTx_BDH (see Figure 19) and the status register UARTx_S2 (see Figure 22).

Bit	7	6	5	4	3	2	1	0
Read	LBKDIE	RXEDGIE	SBNS					
Write								
Reset	0	0	0	0	0	0	0	0

Figure 19. UARTx_BDH register differences

The UART2 module on the KL43/KL33/KL27/KL17 MCUs does not support the module control in the Wait mode. Therefore, the DOZE mode enable is removed from the UART2 control register UARTx_C1 (see Figure 20).

Bit	7	6	5	4	3	2	1	0
Read	LOOPS	DOZEEN	RSRC	M	WAKE	ILT	PE	PT
Write								
Reset	0	0	0	0	0	0	0	0

Figure 20. UARTx_C1 register differences

The flags in the status register UARTx_S1 cannot be cleared by writing 1 to them (see Figure 21). A detailed description of the flag-clearing mechanism is provided in the corresponding reference manual.

Bit	7	6	5	4	3	2	1	0
Read	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
Write				w1c	w1c	w1c	w1c	w1c
Reset	1	1	0	0	0	0	0	0

Figure 21. UARTx_S1 register differences

Bit	7	6	5	4	3	2	1	0
Read	LBKDIF	RXEDGIF	MSBF	RXINV	RWUID	BRK13	LBKDE	RAF
Write								
Reset	0	0	0	0	0	0	0	0

Figure 22. UARTx_S2 register differences

The UART2 module on the KL43/KL33/KL27/KL17 MCUs does not support the 10-bit data mode, as opposed to the UART0 module on the KLx6/KL34 MCUs. Only the 9-bit data mode is available.

The ninth bit of the received data is read from the ninth bit of the UARTx_C3 control register. For a 9-bit transfer, write the ninth data bit into the sixth bit of the UARTx_C3 control register. The UARTx_C3 control register of the UART on the KL43/KL33/KL27/KL17 MCUs and the UART1/UART2 on the KLx6/KL34 MCUs are equivalent.

Bit	7	6	5	4	3	2	1	0
Read	R8T9	R9T8	TXDIR	TXINV	ORIE	NEIE	FEIE	PEIE
Write								
Reset	0	0	0	0	0	0	0	0

Figure 23. UARTx_C3 register differences (versus UART0_C3 on KLx6/KL34)

The UART2 module on the KL43/KL33/KL27/KL17 MCUs does not support the 10-bit data mode, as opposed to the UART0 module on the KLx6/KL34 MCUs. The M10 field in the UARTx_C4 control register represents the position of the parity bit. When set, the parity bit is represented by the tenth bit in the serial transmission. The baud-rate generator used in the UART2 module on the KL43/KL33/KL27/KL17 MCUs is different from the UART0/UART1/UART2. It includes five bits of fine adjustment (fractional segment $BRFD = 32/BRFA$), available as the BRFA field in the UARTx_C4 control register. The baud-rate calculation differences between the UART2 module available on the KL43/KL33/KL27/KL17 MCUs and the UART0/UART1/UART2 modules available on the KLx6/KL34 MCUs are listed in this table:

Table 7. UART_C4 register differences

KLx6/KL34		KL43/KL33/KL27/KL17
UART0	UART1/UART2	UART2
$\text{baud rate} = \frac{\text{UART clock}}{((\text{OSR} + 1) \times \text{SBR}[12:0])}$	$\text{baud rate} = \frac{\text{UART clock}}{(16 \times \text{SBR}[12:0])}$	$\text{baud rate} = \frac{\text{UART clock}}{(16 \times (\text{SBR}[12:0] + \text{BRFA}/32))}$

NOTE

The UART1/UART2 modules on the KLx6/KL34 MCUs have the UARTx_C4 control register, which is equivalent to the UARTx_C5 control register in the UART module on the KL43/KL33/KL27/KL17 MCUs.

Bit	7	6	5	4	3	2	1	0
Read	MAEN1	MAEN2	M10	BRFA				
Write								
Reset	0	0	0					

Figure 24. UARTx_C4 register differences

The UART2 module on the KL43/KL33/KL27/KL17 MCUs does not support the rising- and falling-edge sampling by the receiver, as well as the control of the resynchronization during the data word reception. This feature is removed, as shown in the following figure.

Bit	7	6	5	4	3	2	1	0
Read	TDMAE	0	RDMAE	0	0	0	BOTHEDGE	RESYNCDI
Write								S
Reset	0	0	0	0	0	0	0	0

Figure 25. UARTx_C5 register differences

All additional differences are related to the new features that are available only on the UART2 module on the KL43/KL33/KL27/KL17 MCUs (such as ISO7816) and do not affect the migration from the KLx46/KL34 MCUs.

5.8.1 Software impact

Consider all previously-mentioned differences when migrating from the KLx6/KL34 MCUs to the KL43/KL33/KL27/KL17 MCUs.

5.8.2 Hardware impact

There is no hardware impact when using the updated UART module.

5.9 I²C module update

The main change to the I²C module available on the KL43/KL33/KL27/KL17 MCUs is a higher communication rate due to the double-buffering support (which is not supported on the KLx6/KL34 MCUs). The interface is designed to operate at up to 400 kbit/s, as opposed to the maximum of 100 kbit/s available on the KLx6/KL34 MCUs.

The first difference is in the status register. The I²C module on the KL43/KL33/KL27/KL17 MCUs has an extended number of status flags, which results in two status registers (I2Cx_S1 and I2Cx_S2). The I2Cx_S1 status register is identical to the I2Cx_S status register implemented on the KLx6/KL34 MCUs (with the same address offset). The I2Cx_S2 status register (see the following figure) includes the status flags related to the double-buffering feature. The buffer empty (EMPTY) and the buffer read/write error (ERROR) flags are implemented.

Bit	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	ERROR	EMPTY
Write							w1c	
Reset	0	0	0	0	0	0	0	1

Figure 26. New register I2Cx_S2

The I²C module on the KL43/KL33/KL27/KL17 MCUs supports both the start and stop flag detection with a shared interrupt control. The start flag detection is not available on the KLx6/KL34 MCUs. The input glitch filter register is updated with this feature on the KL43/KL33/KL27/KL17 MCUs (see the following figure). However, this feature reduces the number of bits available for the filter factor. Therefore, you may configure only up to 15 module clock cycles for a glitch width, as opposed to 32 bus cycles on the KLx6/KL34 MCUs.

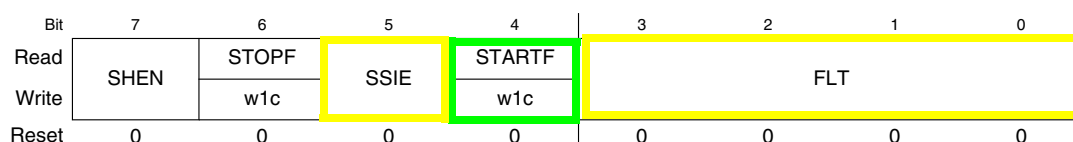


Figure 27. I2Cx_FLT register update

Table 8. I²C module clocks (KL43/KL33/KL27/KL17 versus KLx6/KL34 pinouts)

Module	KLx6/KL34	KLx3
	Clock	Clock
I ² C0	Bus clock	System clock
I ² C1	System clock	System clock

NOTE

The I²C1 module on the KL43/KL33/KL27/KL17 MCUs does not support the high drive capability of the I²C1 pads.

5.9.1 Software impact

There is a significant software impact due to the double-buffering feature. Look at the double-buffering mode section and the flowchart related to the I²C interrupt routine at the end of the I²C module section in the corresponding MCU reference manual.

Consider these notes:

- Check the EMPTY status flag before writing to the I2C_D register and wait for the EMPTY flag to write the second value to the I2C_D immediately after the first write (to apply the double-buffering feature).
- The master must send the NACK before the repeat start in the buffering mode.
- The I²C module on the KLx6/KL34 MCUs must wait for the I2C_D register to be read to start the next transaction. With the KL43/KL33/KL27/KL17 I²C module in the buffer mode, the TCF is cleared automatically by the internal reading or writing into the I2C_D data register. You don't have to wait to read from/write to the I²C data register manually in the Rx/Tx mode.
- A delay is required during the repeated start sequence due to the EMPTY flag. Send the repeat start, apply a small delay (depends on the I²C clock selection) before waiting for the EMPTY flag, and then write to the I2C_D register.

5.9.2 Hardware impact

There is no hardware impact.

5.10 USB module

The USB module on the KL43/KL33/KL27/KL17 MCUs supports full-speed (FS) devices only. All features related to the host (OTG) supported by the KLx6/KL34 MCUs are removed (see [Figure 28–Figure 33](#)).

The highest advantage of the USB module available on the KL43/KL33/KL27/KL17 MCUs is the clock-recovery feature for the crystal-less solution, which you may configure using these USB clock-recovery registers:

- USBx_CLK_RECOVER_CTRL control register.
- USBx_CLK_RECOVER_IRC_EN enable register.
- USBx_CLK_RECOVER_INT_EN interrupt enable register.
- USBx_CLK_RECOVER_INT_STATUS interrupt status register.

The USB module enables the FS USB controller to work with the HIRC 48-MHz clocks, whose accuracy is $\pm 1.5\%$ after the factory trim. This feature is not supported on the KLx6/KL34 MCUs.

NOTE

The clock-recovery feature is only available when the USB works in the full-speed device mode.

The keep-alive is a new feature that is available only on the KL43/KL33/KL27/KL17 MCUs. This feature enables the USB module to be active in the STOP/VLPS modes. There is no need to re-enumerate when exiting the low-power modes. Configure this feature using these two registers:

- USBx_KEEP_ALIVE_CTRL keep-alive mode control register.
- USBx_KEEP_ALIVE_WKCTRL wake-up control register.

NOTE

The keep-alive feature with the USB RAM is not included on the KL43/KL33/KL27/KL17 MCUs with 128/256 KB flash memory (only on MCUs with 32/64 KB flash memory).

Bit	7	6	5	4	3	2	1	0
Read	DPHIGH	0	DPLOW	DMLOW	0	OTGEN	0	0
Write								
Reset	0	0	0	0	0	0	0	0

Figure 28. Eliminated bit fields in control register USBx_CTL0 vs. USBx_OTGCTL

Bit	7	6	5	4
Read	JSTATE	SE0	TXSUSPENDTOKENB	RESET
Write			USY	
Reset	0	0	0	0

Bit	3	2	1	0
Read	HOSTMODEEN	RESUME	ODDRST	USBENSOFEN
Write				
Reset	0	0	0	0

Figure 29. Eliminated bit fields in control register USBx_CTL1 vs. USBx_CTL

Bit	7	6	5	4	3	2	1	0
Read	LSEN				ADDR			
Write								
Reset	0	0	0	0	0	0	0	0

Figure 30. Eliminated bit fields in address register USBx_ADDR

Bit	7	6	5	4	3	2	1	0
Read	HOSTWOH		0	EPCTLDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Write	UB							
Reset	0	0	0	0	0	0	0	0

Figure 31. Eliminated bit fields in endpoint control register USBx_ENDPTn

Bit	7	6	5	4	3	2	1	0
Read	STALL	ATTACH	RESUME	SLEEP	TOKDNE	SOFTOK	ERROR	USBRST
Write	w1c		w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0

Figure 32. Eliminated bit fields in interrupt status register USBx_ISTAT

Bit	7	6	5	4	3	2	1	0
Read	STALLN	ATTACHEN	RESUMEEN	SLEEPEN	TOKDNEEN	SOFTOKEN	ERROREN	USBRSTEN
Write								
Reset	0	0	0	0	0	0	0	0

Figure 33. Eliminated bit fields in interrupt enable register USBx_INTEN

5.10.1 Software impact

Consider all previously-mentioned features. The USB host is not supported on the KL43/KL33/KL27/KL17 MCUs. The USB device has minimal impact on the software because all features related to the MCU are included.

5.10.2 Hardware impact

There is no hardware impact when using the USB module.

5.11 SLCD module differences

The KL43/KL33/KL27/KL17 MCUs support smaller segment SLCDs. The KL43/KL33/KL27/KL17 MCUs can generate only eight back-plane signals and 47 front-plane signals. The KLx6/KL34 MCUs include eight back planes and 63 front planes.

5.11.1 Software impact

Consider the previously-mentioned feature when migrating software. When using up to 8×47 planes, there is no software impact. However, when using a segment display bigger than 8×47 (4×51) on the KLx6/KL34 MCUs, you have to completely reconfigure the module. Considering that the maximum package available for the KL43/KL33/KL27/KL17 MCUs is 64LQFP (BGA), there is no software impact.

5.11.2 Hardware impact

When using a higher-volume segment display, handle the pin-related planes that are not available on the device appropriately. Considering that the maximum package available for the KL43/KL33/KL27/KL17 MCUs is 64LQFP (BGA), there is no hardware impact.

6 Removed Modules

6.1 TSI module

The TSI module is removed on the KL43/KL33/KL27/KL17 MCUs. Use the software touch-sensing methods (TSS or FT based on the GPIO, etc.).

6.1.1 Software impact

Remove all software related to the TSI module. If using the TSS (FT) library on the KLx6/KL34 MCUs, replace the TSI method by a GPIO method on the KL43/KL33/KL27/KL17 MCUs.

6.1.2 Hardware impact

If using a GPIO method based on the TSS (FT), the impact is lower. However, you must make considerable changes related to the GPIO method principle.

6.2 VREG module (on KL43/KL33/KL27/KL17 with 32/64 KB flash)

The USB voltage regulator (VREG) module is not included on the KL43/KL33/KL27/KL17 MCUs with 32/64 KB flash memory. The VREGIN pin is replaced by the PTE16 (with ADC, GPIO, SPI_PCS0, UART2_TX, TPM_CLKIN0, and FXIO0_D0 functionalities) and the VOUT33 pin is replaced by the USB_VDD functionality.

6.2.1 Software impact

There is no software impact. Writing the adequate bit fields to the SIM_SOPT1 (excluding SIM_SOPT1CFG) does not have any effect.

6.2.2 Hardware impact

If not using the VREG and USB modules, there is no impact. Connect the VREGIN and VOUT33 pins together and tie them to the GND using a 10-k Ω resistor (it is not possible to use the PTE16 on the KL43/KL33/KL27/KL17 MCUs with 32/64 KB flash).

If you use the USB regulator, then there is a significant hardware impact because the MCU is not powered properly by the VOUT33 (USB_VDD). There is also a significant hardware impact because the VREGIN pin with a maximum voltage specification of 5.5 V is replaced by the general analog/digital PTE16 pin. This can cause damage because there is no current limitation available. Disconnect the PTE16 (VREGIN) pin from the external 5 V power supply and connect the external 3.3 V power supply to the USB_VDD (VOUT33) pin.

7 Appendices

7.1 Pin multiplexing

The table below shows the pin multiplexing differences between the KL43 and KL46 MCUs in the same 64LQFP package. This section focuses on the reuse of hardware between the MCUs. The table uses these conventions:

Color key	
GREEN	Designates new additions
RED	Designates removals

Table 9. KL43 versus KL46 pinouts

64 LQFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	PTE0	DISABLE D	LCD_P48	PTE0/CLKOUT32K	SPI1_MISO	UART1_TX	RTC_CLKOUT	CMP0_OUT	I2C1_SDA	LCD_P48
2	PTE1	DISABLE D	LCD_P49	PTE1	SPI1_MOSI	UART1_RX	—	SPI1_MISO	I2C1_SCL	LCD_P49
3	VDD	VDD	VDD	—	—	—	—	—	—	—
4	VSS	VSS	VSS	—	—	—	—	—	—	—
5	USB0_DP	USB0_DP	USB0_DP	—	—	—	—	—	—	—
6	USB0_DM	USB0_DM	USB0_DM	—	—	—	—	—	—	—
7 ¹	VOUT33	VOUT33	VOUT33	—	—	—	—	—	—	—
8 ²	VREGIN	VREGIN	VREGIN	—	—	—	—	—	—	—
9	PTE20	ADC0_DP0/ADC0_SE0	LCD_P59/ADC0_DP0/ADC0_SE0	PTE20	—	TPM1_CH0	UART0_TX	—	FXIO0_D4	LCD_P59
10	PTE21	ADC0_DM0/ADC0_SE4a	LCD_P60/ADC0_DM0/ADC0_SE4a	PTE21	—	TPM1_CH1	UART0_RX	—	FXIO0_D5	LCD_P60
11	PTE22	ADC0_DP3/ADC0_SE3	ADC0_DP3/ADC0_SE3	PTE22	—	TPM2_CH0	UART2_TX	—	FXIO0_D6	—
12	PTE23	ADC0_DM3/ADC0_SE7a	ADC0_DM3/ADC0_SE7a	PTE23	—	TPM2_CH1	UART2_RX	—	FXIO0_D7	—
13	VDDA	VDDA	VDDA	—	—	—	—	—	—	—

Table 9. KL43 versus KL46 pinouts (continued)

14	VREFH	VREFH/VREF_OUT	VREFH/VR EF_OUT	—	—	—	—	—	—	—
15	VREFL	VREFL	VREFL	—	—	—	—	—	—	—
16	VSSA	VSSA	VSSA	—	—	—	—	—	—	—
17	PTE29	CMP0_IN5/ADC0_SE4b	CMP0_IN5/ADC0_SE4b	PTE29	—	TPM0_C H2	TPM_CLK IN0	—	—	—
18 ³	PTE30	DAC0_OUT/ADC0_SE23/CMP0_IN4	DAC0_OUT/ADC0_SE23/CMP0_IN4	PTE30	—	TPM0_C H3	TPM_CLK IN1	—	—	—
19	PTE31	DISABLED	—	PTE31	—	TPM0_C H4	—	—	—	—
20	PTE24	DISABLED	—	PTE24	—	TPM0_C H0	—	I2C0_SCL	—	—
21	PTE25	DISABLED	—	PTE25	—	TPM0_C H1	—	I2C0_SDA	—	—
22	PTA0	SWD_CLK	TSI0_CH1	PTA0	—	TPM0_C H5	—	—	—	SWD_CLK
23	PTA1	DISABLED	TSI0_CH2	PTA1	UART0_RX	TPM2_C H0	—	—	—	—
24	PTA2	DISABLED	TSI0_CH3	PTA2	UART0_TX	TPM2_C H1	—	—	—	—
25	PTA3	SWD_DIO	TSI0_CH4	PTA3	I2C1_SCL	TPM0_C H0	—	—	—	SWD_DIO
26	PTA4	NMI_b	TSI0_CH5	PTA4	I2C1_SDA	TPM0_C H1	—	—	—	NMI_b
27	PTA5	DISABLED	—	PTA5	USB_CLKIN	TPM0_C H2	—	—	I2S0_TX_BCLK	—
28	PTA12	DISABLED	—	PTA12	—	TPM1_C H0	—	—	I2S0_TXD0	—
29	PTA13	DISABLED	—	PTA13	—	TPM1_C H1	—	—	I2S0_TX_FS	—
30	VDD	VDD	VDD	—	—	—	—	—	—	—
31	VSS	VSS	VSS	—	—	—	—	—	—	—
32	PTA18	EXTAL0	EXTAL0	PTA18	—	UART1_RX	TPM_CLK IN0	—	—	—
33	PTA19	XTAL0	XTAL0	PTA19	—	UART1_TX	TPM_CLK IN1	—	LPTMR0_ALT1	—
34	PTA20	RESET_b	—	PTA20	—	—	—	—	—	RESET_b

Table 9. KL43 versus KL46 pinouts (continued)

35	PTB0/LLWU_P5	LCD_P0/ ADC0_SE8/ TSIO_C H0	LCD_P0/A DC0_SE8/ TSIO_CH0	PTB0/LLWU_P5	I2C0_SCL	TPM1_CH0	—	—	—	LCD_P0
36	PTB1	LCD_P1/ ADC0_SE9/ TSIO_C H6	LCD_P1/A DC0_SE9/ TSIO_CH6	PTB1	I2C0_SDA	TPM1_CH1	—	—	—	LCD_P1
37	PTB2	LCD_P2/ ADC0_SE12/ TSIO_CH7	LCD_P2/A DC0_SE12/ TSIO_CH7	PTB2	I2C0_SCL	TPM2_CH0	—	—	—	LCD_P2
38	PTB3	LCD_P3/ ADC0_SE13/ TSIO_CH8	LCD_P3/A DC0_SE13/ TSIO_CH8	PTB3	I2C0_SDA	TPM2_CH1	—	—	—	LCD_P3
39	PTB16	LCD_P12/ TSIO_CH9	LCD_P12/ TSIO_CH9	PTB16	SPI1_MOSI	UART0_RX	TPM_CLKIN0	SPI1_MISO	—	LCD_P12
40	PTB17	LCD_P13/ TSIO_CH10	LCD_P13/ TSIO_CH10	PTB17	SPI1_MISO	UART0_TX	TPM_CLKIN1	SPI1_MOSI	—	LCD_P13
41	PTB18	LCD_P14/ TSIO_CH11	LCD_P14/ TSIO_CH11	PTB18	—	TPM2_CH0	I2S0_TX_BCLK	—	—	LCD_P14
42	PTB19	LCD_P15/ TSIO_CH12	LCD_P15/ TSIO_CH12	PTB19	—	TPM2_CH1	I2S0_TX_FS	—	—	LCD_P15
43	PTC0	LCD_P20/ ADC0_SE14/ TSIO_CH13	LCD_P20/A DC0_SE14/ TSIO_CH13	PTC0	—	EXTRG_IN	audioUSB_SOF_OUT	CMP0_OUT	I2S0_TX_D0	LCD_P20
44	PTC1/LLWU_P6/RTC_CLKIN	LCD_P21/ ADC0_SE15/ TSIO_CH14	LCD_P21/A DC0_SE15/ TSIO_CH14	PTC1/LLWU_P6/RTC_CLKIN	I2C1_SCL	—	TPM0_CH0	—	I2S0_TX_D0	LCD_P21
45	PTC2	LCD_P22/ ADC0_SE11/ TSIO_CH15	LCD_P22/A DC0_SE11/ TSIO_CH15	PTC2	I2C1_SDA	—	TPM0_CH1	—	I2S0_TX_FS	LCD_P22
46	PTC3/LLWU_P7	LCD_P23	LCD_P23	PTC3/LLWU_P7	SPI1_SCK	UART1_RX	TPM0_CH2	CLKOUT	I2S0_TX_BCLK	LCD_P23
47	VSS	VSS	VSS	—	—	—	—	—	—	—
48	VLL3	VLL3	VLL3	—	—	—	—	—	—	—
49	VLL2	VLL2	VLL2/LCD_P4	PTC20	—	—	—	—	—	LCD_P4

Table 9. KL43 versus KL46 pinouts (continued)

50	VLL1	VLL1	VLL1/LCD_P5	PTC21	—	—	—	—	—	LCD_P5
51	VCAP2	VCAP2	VCAP2/LCD_P6	PTC22	—	—	—	—	—	LCD_P6
52	VCAP1	VCAP1	VCAP1/LCD_P39	PTC23	—	—	—	—	—	LCD_P39
53	PTC4/LLWU_P8	LCD_P24	LCD_P24	PTC4/LLWU_P8	SPI0_PCS0	UART1_TX	TPM0_CH3	I2S0_MCLK	—	LCD_P24
54	PTC5/LLWU_P9	LCD_P25	LCD_P25	PTC5/LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0	—	CMP0_OUT	LCD_P25
55	PTC6/LLWU_P10	LCD_P26/CMP0_IN0	LCD_P26/CMP0_IN0	PTC6/LLWU_P10	SPI0_MOSI	EXTRG_IN	I2S0_RX_BCLK	SPI0_MISO	I2S0_MCLK	LCD_P26
56	PTC7	LCD_P27/CMP0_IN1	LCD_P27/CMP0_IN1	PTC7	SPI0_MISO	audioUSB_SOF_OUT	I2S0_RX_FS	SPI0_MOSI	—	LCD_P27
57	PTD0	LCD_P40	LCD_P40	PTD0	SPI0_PCS0	—	TPM0_CH0	—	FXI00_D0	LCD_P40
58	PTD1	LCD_P41/ADC0_SE5b	LCD_P41/ADC0_SE5b	PTD1	SPI0_SCK	—	TPM0_CH1	—	FXI00_D1	LCD_P41
59	PTD2	LCD_P42	LCD_P42	PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO	FXI00_D2	LCD_P42
60	PTD3	LCD_P43	LCD_P43	PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI	FXI00_D3	LCD_P43
61	PTD4/LLWU_P14	LCD_P44	LCD_P44	PTD4/LLWU_P14	SPI1_PCS0	UART2_RX	TPM0_CH4	—	FXI00_D4	LCD_P44
62	PTD5	LCD_P45/ADC0_SE6b	LCD_P45/ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5	—	FXI00_D5	LCD_P45
63	PTD6/LLWU_P15	LCD_P46/ADC0_SE7b	LCD_P46/ADC0_SE7b	PTD6/LLWU_P15	SPI1_MOSI	UART0_RX	—	SPI1_MISO	FXI00_D6	LCD_P46
64	PTD7	LCD_P47	LCD_P47	PTD7	SPI1_MISO	UART0_TX	—	SPI1_MOSI	FXI00_D7	LCD_P47

¹ The VOUT33 pin on the KL43/KL33/KL27/KL17 MCUs with 32/64 KB flash is replaced by the USB_VDD. These devices do not include the USB voltage regulator. If using the USB module, power the USB_VDD from an external 3.3 V power supply.

² The VREGIN pin on the KL43/KL33/KL27/KL17 MCUs with 32/64KB flash is replaced by a general-functionality analog/digital pin PTE16. These devices do not include the USB voltage regulator. Do not connect a 5 V power supply to this pin for these MCUs.

³ The VREF_OUT pin is shared with the PTE30 pin on the KL43/KL33/KL27/KL17 MCUs with 32/64 KB flash on 36-pin (and lower) packages.

8 References

These resources are available on www.nxp.com:

- KL46 Sub-Family Reference Manual (document [KL46P121M48SF4RM](#))
- KL46 Sub-Family Data Sheet (document [KL46P121M48SF4](#))
- [Kinetis L Series MCUs](#)

9 Revision History

This table summarizes the changes made to this document since the initial release:

Table 10. Revision history

Revision number	Date	Substantive changes
0	09/2014	Initial release.
1	04/2016	• Updated Section 1, "Introduction". • Updated the differences between the KL43/KL33/KL27/KL17 MCUs with different flash sizes (devices with 128/256 KB flash are different from devices with 32/64 KB flash), corrected the DAC, VREG, and VREF_OUT pin assignment. • Updated the differences between the KL43/KL33/KL27/KL17 MCUs with different packages (48/64-pin packages are different from the 32/36-pin packages), especially the VREF_OUT assignment. • Added the new CRC module available on the KL43/KL33/KL27/KL17 MCUs with 32/64 KB flash. • Updated the I²C module software impact. • Updated the USB keep-alive feature.

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