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Application Note

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A Guide to Transitioning from the MPC556x to the MPC5644A

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1 Introduction

This document provides a summary of the differences between Freescale's MPC556x family of devices and the MPC5644A, and may be used as an aid for planning a migration to the MPC5644A.

The MPC5644A is available in 324 BGA, 208 BGA, and 176 QFP packages. This guide will only discuss the migration between the MPC556x and MPC5644A with respect to the 324 BGA package.

Contents

2 Overview

Table 1 provides a summary of the feature differences between the MPC556x and MPC5644A devices.

Table 1. MPC556x/MPC5644A feature comparison

Feature	MPC5565	MPC5566	MPC5644A
Process	130 nm	130 nm	90 nm
Core	e200z6	e200z6	e200z4
SIMD / SPE	Yes	Yes	Yes
VLE	Yes	Yes	Yes
Cache	8 KB Unified	32 KB Unified	8 KB Instruction only
Non-maskable interrupt (NMI)	No	No	NMI and critical interrupt
MMU	32 entry	32 entry	24 entry
Memory protection unit (MPU)	No	No	Yes
XBAR	3×5	4×5	5×4
Windowing software watchdog	No	No	Yes
Core Nexus	3+	3+	3+
SRAM	64 KB	128 KB	192 KB
Flash	2 MB	3 MB	4 MB
Flash fetch accelerator	2 × 256 bit	2 × 256 bit	4 × 256 bit
External bus	16-bit	32-bit	16-bit non-muxed 32-bit muxed
Calibration bus	16-bit	16-bit	16-bit non-muxed 32-bit muxed
DMA	32 channels	64 channels	64 channels
DMA Nexus	Class 3	Class 3	No
Serial	2	2	3
eSCI_A	Yes	Yes	Yes (MSC uplink)
eSCI_B	Yes	Yes	Yes (MSC uplink)
eSCI_C	No	No	Yes
FlexCAN	3	4	3
CAN_A	64 buf	64 buf	64 buf
CAN_B	64 buf	64 buf	64 buf
CAN_C	64 buf	64 buf	64 buf
CAN_D	No	64 buf	No
SPI	3	4	3
DSPI_A	No	Yes	No
DSPI_B	Yes	Yes	Yes (MSC support)
DSPI_C	Yes	Yes	Yes (MSC support)
DSPI_D	Yes	Yes	Yes
Microsecond bus downlink	No	No	Yes
FlexRay	No	No	Yes
Ethernet	No	Yes	No
System timers	No	No	5 PIT chan 4 Compares 1 Watchdog
eMIOS	24 channels	24 channels	24 channels
eTPU	32 channels	64 channels	32 channels
eTPU_A	Yes	Yes	Yes (eTPU2)

Table 1. MPC556x/MPC5644A feature comparison (continued)

Feature	MPC5565	MPC5566	MPC5644A
eTPU_B	No	Yes	No
Code memory	12 KB	20 KB	14 KB
Data memory	2.5 KB	4 KB	3 KB
Reaction module	No	No	6 channels
Interrupt controller	210 channels	308 channels	476 channels
eQADC	40 channels, 2 ADCs	40 channels, 2 ADCs	40 channels, 2 ADCs
Temperature sensor	No	No	Yes
Variable gain amp.	No	No	Yes
Decimation filter	No	No	Yes × 2
Sensor diagnostics	No	No	Yes
PLL	FM	FM	FM
CRC	No	No	Yes
VRC	Yes	Yes	Yes
PMC	No	No	Yes
Supplies	5 V, 3.3 V, 1.5	5 V, 3.3 V, 1.5V	5 V, 3.3 V, 1.2V
Low power modes	No	No	Stop mode Slow mode

There are both hardware and software considerations that need to be made when migrating from an MPC556x device to the MPC5644A. This document details software and hardware compatibility considerations, along with new features that have been implemented on the MPC5644A. The following topics are covered:

Hardware considerations

- Section 3.1, “Ball map: hardware compatibility”
- Section 3.2, “Boot configuration: hardware compatibility”
- Section 3.3, “PLL configuration: hardware compatibility”
- Section 3.4, “Clock circuitry: hardware compatibility”
- Section 3.5, “Power supplies”

Software considerations

- Section 4.1, “System modules”
- Section 4.2, “e200z4 Core”
- Section 4.3, “Internal/external memory”
- Section 4.4, “Analog”
- Section 4.5, “Timer modules”
- Section 4.6, “Communication peripherals”
- Section 4.7, “Nexus and JTAG (debug)”
- Section 4.8, “Power management controller (PMC)”

3 Hardware considerations

3.1 Ball map: hardware compatibility

The 324 BGA ball maps of the MPC5565 and the MPC5644A are shown respectively in Figure A-1 and Figure A-2 in Appendix A, "Ball map diagrams."

The ball maps of the 324 BGA production packages of the MPC556x and MPC5644A devices are not pin-to-pin compatible. Existing MPC556x hardware will have to be modified for the MPC5644A.

A level of compatibility has been maintained within the location of signal groups, whereby the orientation of signal groups is similar between the two devices (for example, eMIOS is on the bottom row right-hand side, etc.). This is aimed at reducing the need to relocate components on existing MPC556x hardware.

The one notable exception to the compatibility in signal groups is the reduced port Nexus signals (MDO0–3, etc.). It is recommended that these be routed within the space between the outer ring and inner balls, then taken out via the top right corner (illustrated in Figure 1). This will allow them to route out in a similar position to the MPC556x device.

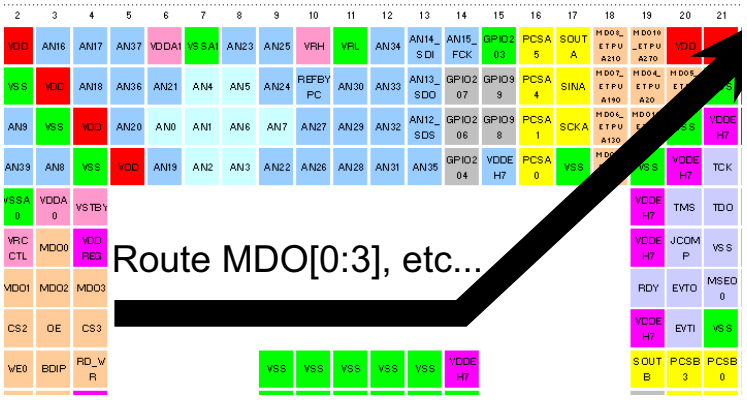


Figure 1. Compatible routing of Nexus signals

3.2 Boot configuration: hardware compatibility

The differences in the boot configuration pins, BOOTCFG[0:1], are shown in Table 2.

Table 2. BOOTCFG[0:1] configuration

Value	MPC556x	MPC5644A
0b00	Boot from internal memory	Boot from internal memory
0b01	FlexCAN / eSCI boot	FlexCAN / eSCI boot
0b10	Boot from external memory (no arbitration)	Boot from external memory (no arbitration)
0b11	Boot from external memory (external arbitration)	Reserved

The signals WKPCFG, RSTCFG, RESET, and RSTOUT have the same functionality in both devices.

3.3 PLL configuration: hardware compatibility

The configuration of the PLL configuration pins is different between the MPC556x and the MPC5644A.

The clock configuration for the MPC556x devices is shown in Table 3. In this configuration, the PLLCFG0 and PLLCFG1 pins are used to determine the clock mode.

Table 3. MPC556x PLL configuration

PLLCFG0	PLLCFG1	MPC556x clock mode
0	0	Bypass mode
0	1	External reference
1	0	Crystal reference
1	1	Dual controller mode

On the MPC5644A, only one pin is used to determine the clock mode. This is the PLLREF pin shown in Table 4. The clock mode can be changed by software, once out of reset, by using the FMPLL_ESYNCR1 register.

Table 4. MPC5644A PLL configuration

PLLREF	MPC5644A clock mode[1]
0b0	Normal mode with external reference
0b1	Normal mode with crystal reference

1 Clock mode can be changed by software using the FMPLL_ESYNCR1[CLKCFG] register.

The PLLCFG1 pin is used on the 324 TEPBGA package of the MPC5644A to select between two input crystal ranges. The choices available for the PLLCFG1 pin are show in Table 5.

Table 5. MPC5644A External Crystal Range

PLLCFG1	External Crystal Range
0b0	8 MHz to 20 MHz
0b1	16 MHz to 40 MHz

3.4 Clock circuitry: hardware compatibility

The clock circuitry on the MPC556x required a series resistor between the crystal and the XTAL signal. At the time of writing, this is not required on the MPC5644A, but it is recommended to install a 0 Ω resistor to allow for any change to this in the future. This is also the case for the parallel feedback resistor between EXTAL and XTAL. A comparison of the clock circuits is given in Figure 2.

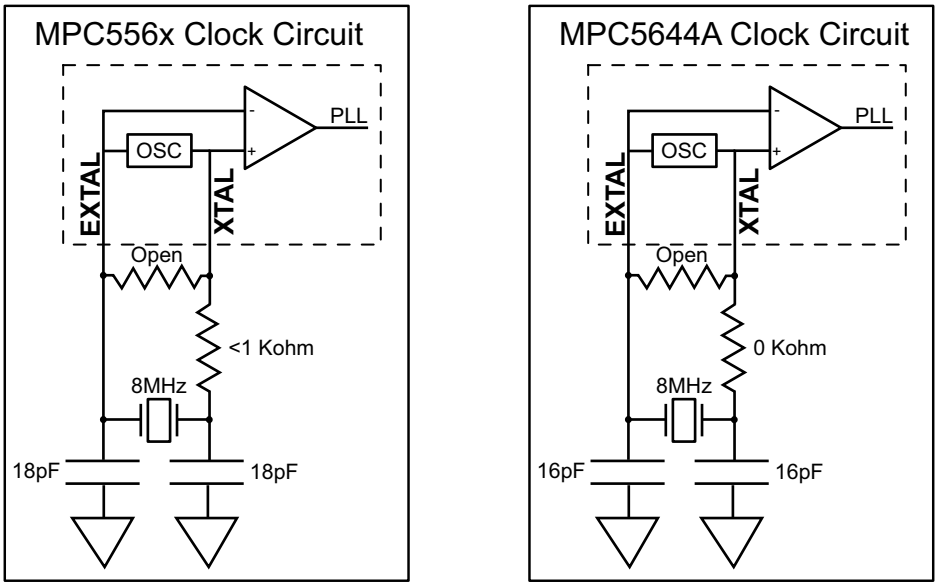


Figure 2. Comparison of clock circuits

NOTE

The same crystal can be used on both devices. If the application is to use FlexRay, then a 40 MHz crystal should be used rather than an 8 MHz crystal.

3.5 Power supplies

3.5.1 Supplies: hardware compatibility

3.5.1.1 Overview

Table 6 details the different options available when evaluating a power supply strategy for the MPC5644A.

Table 6. Overview of the power supply strategy

Function	MPC556x	MPC5644A
VDD supply	1.5 V	1.2 V
• Supports internal regulator supplied	Yes	Yes
• Supports externally supplied	Yes	Yes
Internal 3.3 V regulator	3.3 V	3.3 V
• Supports internal regulator supplied	No	Yes
• Supports externally supplied	Yes	Yes
Supports 5 V operation only	No	Yes

The MPC556x devices implement an internal 1.5 V regulator, but also require both 3.3 V and 5 V external supplies.

In contrast to this, the MPC5644A implements an internal 1.2 V regulator and an internal 3.3 V regulator. If the external bus function is not required (as this function does require an external 3.3 V supply), then the device can powered by a standalone 5 V supply only.

3.5.1.2 Core voltage (VDD)

There is a difference in the nominal voltage supplied to VDD, due to the differences in technology between the devices. Table 7 highlights the nominal voltage for the different devices.

Table 7. Nominal VDD supply

MPC556x nominal VDD	MPC5644A nominal VDD
1.5 V	1.2 V

NOTE

The nominal voltage is used to indicate the voltage required. The actual range of the supply is detailed in the respective device data sheet.

3.5.1.2.1 Externally supplied VDD

As well as the difference in core voltage levels, there is also a difference in the minimum requirements for decoupling on the VDD supply. This is shown in Figure 3.

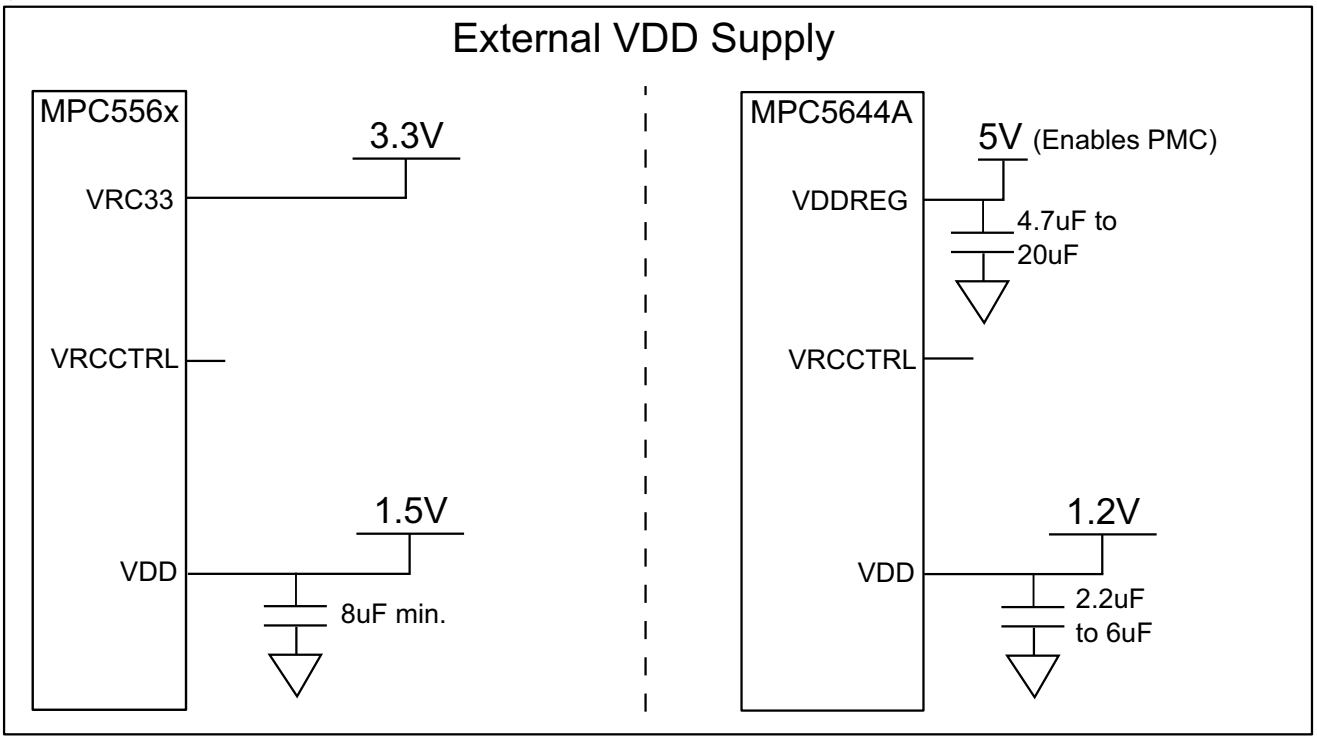


Figure 3. External VDD supply

In Figure 3, the MPC5644A connects VDDREG to 5 V. This powers the power management controller (PMC), which in turn powers the internal regulators. If the internal regulators are not being used it is still recommended to power VDDREG as this also provides programmable LVI functionality on several supplies, including VDD.

3.5.1.2.2 Internally supplied VDD

The internal regulator for the VDD supply uses a similar design, with some slight modifications, between the two devices. This is shown in Figure 4.

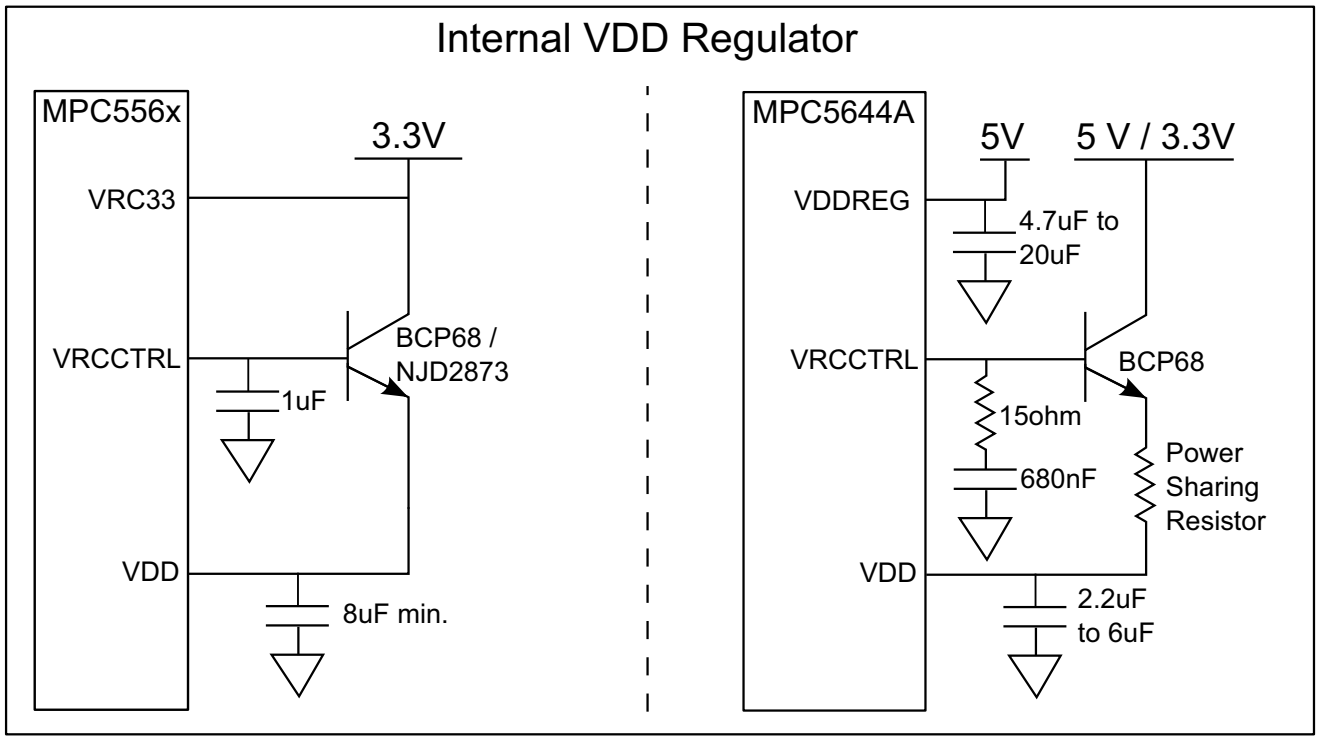


Figure 4. Supplying VDD using the internal VDD regulator

The MPC556x devices specify the use of the BCP68 or NJD2873 dependent upon the current of the device used. The MPC5644A can use either of these transistors; however, the BCP68 is recommended as a cost-effective transistor.

Table 8. Recommended bypass transistor

	MPC5565	MPC5566	MPC5644A
Max core supply current (IDD)[1]	460 mA	820 mA	450 mA
Recommended bypass transistor	BCP68	NJD2873	BCP68

[1] May not be accurate at time of reading. Please refer to device data sheet for guaranteed specifications.

3.5.1.2.3 Using the 1.2 V internal regulator on the MPC5644A

Some care must be taken with component selection when using the 1.2 V internal regulator. The collector voltage for the MPC5644A will typically be 5 V (for systems using only a 5 V supply), which results in more power being dissipated across the bypass transistor.

The following example shows how to determine which bypass transistor to use, and how to calculate the value of a power sharing resistor if required. The parameters used to determine these will vary depending on the system's temperature and frequency requirements.

NOTE

The figures used below (denoted with the character †)are based on expected values. The MPC5644A data sheet should be referred to for the guaranteed specifications.

3.5.1.2.4 MPC5644A example: BCP68 with 5 V supply to bypass transistor

Method

1. Determine the gain requirements of the system.
2. Determine the power requirements of the system.
3. Investigate if a power sharing resistor is required.

Gain

- Maximum transient current (IDD †) = 450 mA
- Minimum base output current (IVRCCTL †) = 11 mA
- Minimum required gain = 450/11 = 36.4

Power

- Steady state MCU current @ 150 MHz (IDD †) = 350mA – 400mA
- Maximum collector voltage = 5V + 5% = 5.25 V
- Minimum emitter voltage = 1.2V – 5% = 1.14 V
- Required power (Pce) = (5.25 V – 1.14 V) × 0.4 A = 1.644 W

The following options are available:

- Use BCP68 with large heat sink area (> 6 cm^2 — please refer to BCP68 data sheet).
- Use BCP68 with power sharing resistor.
- Use NJD2873 (larger package will dissipate more power).

Option 2 — Implementing BCP68 with power sharing resistor

Resistor selection

- Steady state MCU current @ 150 MHz (IDD †) = 350 mA – 400 mA
- Minimum transient supply (supply to collector), minVt = 5 V – 10% = 4.5 V
- Maximum VDD = 1.2 V + 10% = 1.32 V

- Minimum saturation voltage (Vcesat min) = 0.5 V (BCP68 data sheet)
  Add margin to avoid Vce < Vcesat
  — Therefore plan for Vce = 0.7 V
- Minimum emitter voltage (Ve)
  = MinVt –Vce = 4.5 + 0.7
  = 3.8 V
- Maximum resistor value
  = Ve – MaxVDD / IDD = (3.8 – 1.32) / 0.4
  = 6.2 Ω
- Use 5.6 Ω, as commonly available; assume ± 5% tolerance
- Maximum resistor power = $IDD^2 \times (R + 5\%) = 0.4^2 \times (5.6 + 0.28) = 0.941$ W

Temperature considerations

- Maximum external ambient = 125 ºC
- Transistor power maximum
  = (maxVt – minVDD – ((R-5%) × IDD)) × IDD
  = (5.25 – 1.14 – (5.32 × 0.4)) × 0.4 = 0.793 W
- SOT223 (BCP68 package) Tjc (junction to case) = 15 K/W
- FR4 with high thermal density via for SOT223 = 9 K/W
- Heatsink to ambient = 3 K
- Junction temperature = (125 ºC + 3 K) + (15 K/W + 9K/W) × 0.793 W = 147.0 ºC
- Max junction temperature from BCP68 data sheet = 150 ºC
  — Therefore, a 5.6 Ω resistor is a suitable selection to keep temperature within range.

NOTE

The above calculations are directed specifically at the MPC5644A device; however, the methods used are also applicable to the MPC556x devices. Typically on the MPC556x devices the BCP68 collector is supplied by 3.3 V, therefore minimizing Vce, and reducing the requirements for a series resistor.

3.5.1.3 External bus interface supply (EBI)

The supply for the EBI is similar on both devices. The nominal voltage for the EBI supply is 3.3 V. The only caveat is the VDDE-EH supply on the MPC5644A. In a certain configuration, this supply can be used to power GPIO functionality on unused EBI pins, thereby allowing 5 V GPIO. This is shown in Table 9.

Table 9. VDDE-EH supply options

	MPC5644A		
EBI configuration	16-bit non-multiplexed	16-bit multiplexed	32-bit multiplexed
VDDE-EH	3.3 V	5 V / 3.3 V GPIO-dependent	3.3 V

3.5.1.4 eQADC supply filtering

The requirements for filtering the supplies to the eQADC, which are VDDA0, VDDA1,VRH, and REFBYPC, remain the same between the MPC556x and the MPC5644A.

3.5.1.5 Nexus and JTAG supply

The JTAG and Nexus signals use a different scheme for their supply voltages. The implementation on the MPC5644A allows a single 5 V regulator to power the entire device and provide debug access without the requirements for a 3.3 V regulator.

The differences for the JTAG supply are shown in Table 10.

Table 10. JTAG supply requirements

Device	JTAG supply	Nominal voltage	JTAG pin voltage level (TDO, TDI, etc.)
MPC556x	VDDE7	3.3 V	3.3 V
MPC5644A	VDDEH7	5 V	3.3 V

The differences for the Nexus supply are shown in Table 11.

Table 11. Nexus supply requirements

Device	Nexus width	MDO[0:3] supply	Nominal voltage	MDO[4:11] supply	Nominal voltage	Nexus pin voltage level (MDO, etc.)	Max freq
MPC556x	Wide	VDDE7	3.3 V	VDDE7	3.3 V	3.3 V	Fsys / 2
MPC5644A	Narrow	VRC33	3.3 V	—	—	3.3 V	Fsys / 2
MPC5644A	Wide	VRC33	3.3 V	VDDEH7	5 V	3.3 V	Fsys / 4

3.5.1.6 PLL supply

The differences between the two devices' PLL supply are detailed in Table 12.

Table 12. PLL supply differences

Device	PLL supply	Nominal voltage
MPC556x	VDDSYN	3.3 V
MPC5644A	VDDPLL	1.2 V

3.5.2 Supplies: new features

3.5.2.1 Internal 3.3 V regulator

On the MPC556x, the VDD33 supply used an external 3.3 V input to power the internal structures of the device. The VFLASH and VPP supplies also were externally provided to power the flash memory. The MPC5644A combines this functionality onto one supply, VRC33, and allows it to be provided from an external supply or generated from an internal 3.3 V regulator.

Figure 5 illustrates, at a high level, the connections of the VRC33 supply when using both the internal regulator and an external supply. The user must ensure that a decoupling capacitor, ranging between 600 nF and 2 µF, with a low ESR (50 mΩ maximum) is connected to the VRC33.

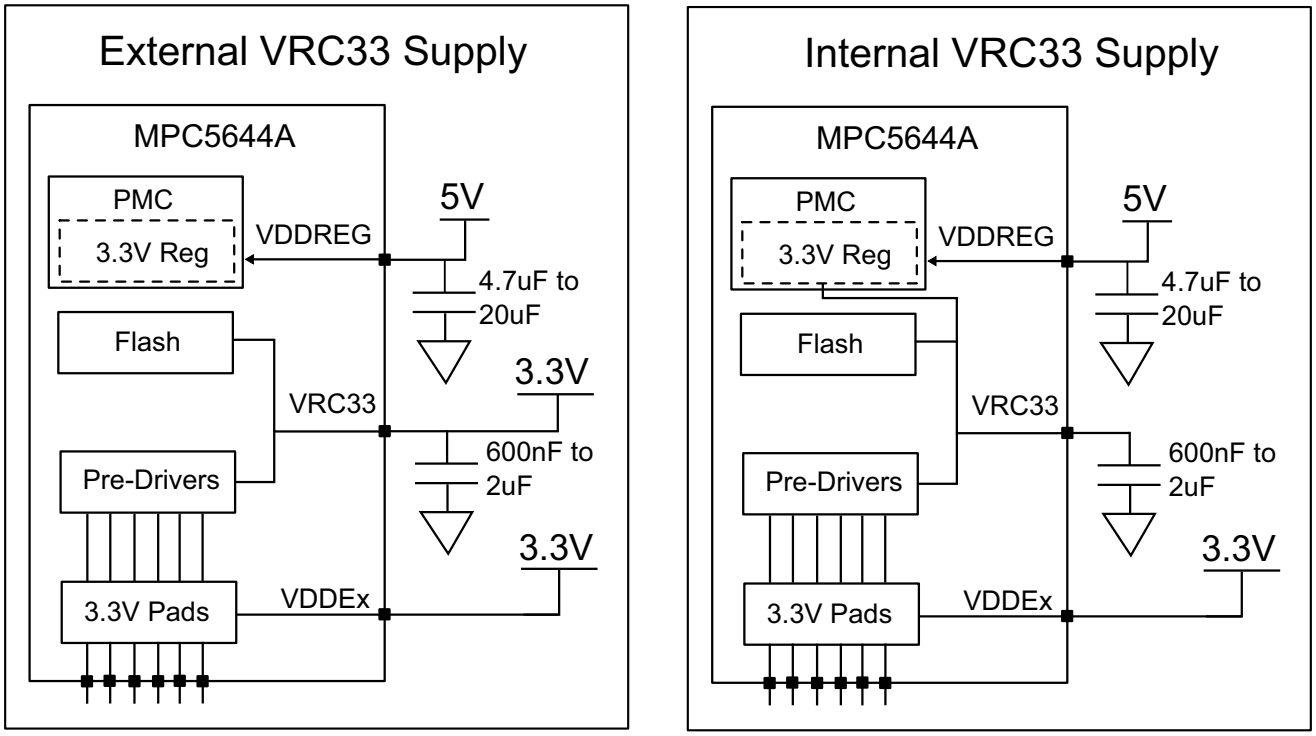


Figure 5. External and internal VRC33 connection

4 Software considerations

4.1 System modules

4.1.1 Boot assist module (BAM)

The boot assist module used on the MPC5644A is based on the MPC556x BAM.

4.1.1.1 BAM: software compatibility

For common features, software written for the MPC556x devices should be compatible with the MPC5644A.

4.1.1.2 BAM: new features

The following features have been implemented on the MPC5644A:

- Baud rate detection for serial boot via SCI or CAN interface
- Support for the software watchdog timer in the reset configuration half-word (RCHW)

The serial boot mode on MPC5644A can run in either of two modes of operation. The state of the EVTO pin during the BAM code execution determines which mode is selected:

- 0 — Standard serial boot mode using fixed baud rates derived from the crystal oscillator
- 1 —Baud rate detection serial boot mode, which allows communication with adaptable speed, based on measured input signal

The status of the EVTO pin is monitored in the SIU_RSR[ABR] bit.

To measure the baud rate of the serial protocol, an empty CAN or eSCI frame must be transmitted from the host, which the BAM uses to determine the correct baud rate being used.

The RCHW has a new Software Watchdog Timer bit implemented. Care must be taken when planning to use the SWT in your application.

If the SWT is disabled in the RCHW, the module will be disabled in the memory space. This does not allow any software access to the SWT and any attempted register accesses will result in an exception.

If you plan to use the SWT in the application, it is recommended that it be enabled in the RCHW, then modified by software after reset to the requirements of the application. If enabled in the RCHW, the SWT can be disabled in software after reset by writing a 0b0 to the SWT_MCR[WEN] bit.

Figure 6 shows the fields of the MPC5644A RCHW.

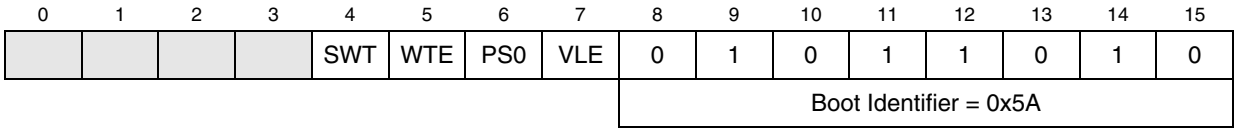


Figure 6. MPC5644A reset configuration half-word (RCHW)

Table 13. RCHW field descriptions

Field	Description
bits 0–3	Reserved. These bit values are ignored when the halfword is read. Write to 0 for future compatibility.
SWT	Watchdog timer enable This bit determines if the software watchdog timer is enabled after passing control to the user application code. 0 Disable software watchdog timer 1 Software watchdog timer maintains its default state out of reset, i.e. enabled. The timeout period is programmed to be 261600 system clocks.
WTE	Device core watchdog timer enable This bit determines if the core software watchdog timer is enabled after passing control to the user application code. 0 Disable core software watchdog timer 1 Software watchdog timer maintains its default state out of reset, in other words enabled. The timeout period is programmed to be 2.5×2^{17} system clocks.
PS0	Port size Defines the width of the data bus connected to the memory on $\overline{CS0}$. After system reset, CS0 is changed to a 16-bit port by the BAM, which fetches the RCHW from either 16- or 32-bit external memories. Then the BAM reconfigures the EBI as a 16-bit bus or a 32-bit bus, according to the settings of this bit. 0 32-bit CS0 port size 1 16-bit CS0 port size
VLE	VLE Code Indicator This bit is used to configure the MMU entries 1-3 coded as either Classic Book E instructions or as Freescale VLE instructions. 0 User code executes as classic Book E code 1 User code executes as Freescale VLE code
BOOTID	Boot identifier This field serves two functions. First, it is used to indicate which block in flash memory contains the boot program. Second, it identifies whether the flash memory is programmed or invalid. The value of a valid boot identifier is 0x5A.

4.1.2 Cyclic redundancy check (CRC)

The MPC5644A implements a cyclic redundancy check module that allows CRC signatures of data to be created in hardware.

4.1.2.1 CRC: software compatibility

The CRC is a new module implemented on the MPC5644A. By default, the CRC is not enabled and requires no changes to existing code.

4.1.2.2 CRC: new features

Two standard generator polynomials for the CRC computation are supported for this operation. These are shown in Equation 1 and Equation 2.

$$\chi^{16} + \chi^{12} + \chi^{5} + 1$$

CRC-CCITT (x25 Protocol) ***Eqn. 1***

$$\chi^{32} + \chi^{26} + \chi^{23} + \chi^{22} + \chi^{16} + \chi^{12} + \chi^{11} + \chi^{10} + \chi^{8} + \chi^{7} + \chi^{5} + \chi^{4} + \chi^{2} + 1$$

CRC-32 (Ethernet Protocol) ***Eqn. 2***

4.1.3 eDMA

The eDMA supports sixty-four channels on the MPC5644A.

4.1.3.1 eDMA: software compatibility

For common modules between these devices, the eDMA channel routing is identical. A comparison of the eDMA sources is shown in Table 14.

Table 14. DMA sources for MPC5644a, MPC5566, and MPC5565

DMA CH	MPC5644A DMA source description	MPC5566 DMA source description	MPC5565 DMA source description
0	eQADC command FIFO 0 fill flag	eQADC command FIFO 0 fill flag	eQADC command FIFO 0 fill flag
1	eQADC receive FIFO 0 drain flag	eQADC receive FIFO 0 drain flag	eQADC receive FIFO 0 drain flag
2	eQADC command FIFO 1 fill flag	eQADC command FIFO 1 fill flag	eQADC command FIFO 1 fill flag
3	eQADC receive FIFO 1 drain flag	eQADC receive FIFO 1 drain flag	eQADC receive FIFO 1 drain flag
4	eQADC command FIFO 2 fill flag	eQADC command FIFO 2 fill flag	eQADC command FIFO 2 fill flag
5	eQADC receive FIFO 2 drain flag	eQADC receive FIFO 2 drain flag	eQADC receive FIFO 2 drain flag
6	eQADC command FIFO 3 fill flag	eQADC command FIFO 3 fill flag	eQADC command FIFO 3 fill flag
7	eQADC receive FIFO 3 drain flag	eQADC receive FIFO 3 drain flag	eQADC receive FIFO 3 drain flag
8	eQADC command FIFO 4 fill flag	eQADC command FIFO 4 fill flag	eQADC command FIFO 4 fill flag
9	eQADC receive FIFO 4 drain flag	eQADC receive FIFO 4 drain flag	eQADC receive FIFO 4 drain flag
10	eQADC command FIFO 5 fill flag	eQADC command FIFO 5 fill flag	eQADC command FIFO 5 fill flag
11	eQADC receive FIFO 5 drain flag	eQADC receive FIFO 5 drain flag	eQADC receive FIFO 5 drain flag
12	DSPIB transmit FIFO fill flag	DSPIB transmit FIFO fill flag	DSPIB transmit FIFO fill flag
13	DSPIB receive FIFO drain flag	DSPIB receive FIFO drain flag	DSPIB receive FIFO drain flag
14	DSPIC transmit FIFO fill flag	DSPIC transmit FIFO fill flag	DSPIC transmit FIFO fill flag

Table 14. DMA sources for MPC5644a, MPC5566, and MPC5565 (continued)

DMA CH	MPC5644A DMA source description	MPC5566 DMA source description	MPC5565 DMA source description
15	DSPIC receive FIFO drain flag	DSPIC receive FIFO drain flag	DSPIC receive FIFO drain flag
16	DSPID transmit FIFO fill flag	DSPID transmit FIFO fill flag	DSPID transmit FIFO fill flag
17	DSPID receive FIFO drain flag	DSPID receive FIFO drain flag	DSPID receive FIFO drain flag
18	eSCIA combined DMA request of the Transmit Data Register Empty, Transmit Complete, and LIN Transmit Data Ready DMA requests	eSCIA combined DMA request of the Transmit Data Register Empty, Transmit Complete, and LIN Transmit Data Ready DMA requests	eSCIA combined DMA request of the Transmit Data Register Empty, Transmit Complete, and LIN Transmit Data Ready DMA requests
19	eSCIA combined DMA request of the Receive Data Register Full and LIN Receive Data Ready DMA requests	eSCIA combined DMA request of the Receive Data Register Full and LIN Receive Data Ready DMA requests	eSCIA combined DMA request of the Receive Data Register Full and LIN Receive Data Ready DMA requests
20	eMIOS channel 0 flag	eMIOS channel 0 flag	eMIOS channel 0 flag
21	eMIOS channel 1 flag	eMIOS channel 1 flag	eMIOS channel 1 flag
22	eMIOS channel 2 flag	eMIOS channel 2 flag	eMIOS channel 2 flag
23	eMIOS channel 3 flag	eMIOS channel 3 flag	eMIOS channel 3 flag
24	eMIOS channel 4 flag	eMIOS channel 4 flag	eMIOS channel 4 flag
25	eMIOS channel 8 flag	eMIOS channel 8 flag	eMIOS channel 8 flag
26	eMIOS channel 9 flag	eMIOS channel 9 flag	eMIOS channel 9 flag
27	eTPUA channel 0 data transfer request status	eTPUA channel 0 data transfer request status	eTPUA channel 0 data transfer request status
28	eTPUA channel 1 data transfer request status	eTPUA channel 1 data transfer request status	eTPUA channel 1 data transfer request status
29	eTPUA channel 2 data transfer request status	eTPUA channel 2 data transfer request status	eTPUA channel 2 data transfer request status
30	eTPUA channel 14 data transfer request status	eTPUA channel 14 data transfer request status	eTPUA channel 14 data transfer request status
31	eTPUA channel 15 data transfer request status	eTPUA channel 15 data transfer request status	eTPUA channel 15 data transfer request status
eDMA channels 32–63 not available on the MPC5565			
32	Reserved	DSPIA transmit FIFO fill flag	N/A
33	Reserved	DSPIA receive FIFO drain flag	N/A
34	eSCIB combined DMA request of the Transmit Data Register Empty, Transmit Complete, and LIN Transmit Data Ready DMA requests	eSCIB combined DMA request of the Transmit Data Register Empty, Transmit Complete, and LIN Transmit Data Ready DMA requests	N/A
35	eSCIB combined DMA request of the Receive Data Register Full and LIN Receive Data Ready DMA requests	eSCIB combined DMA request of the Receive Data Register Full and LIN Receive Data Ready DMA requests	N/A
36	eMIOS channel 6 flag	eMIOS channel 6 flag	N/A

Table 14. DMA sources for MPC5644a, MPC5566, and MPC5565 (continued)

DMA CH	MPC5644A DMA source description	MPC5566 DMA source description	MPC5565 DMA source description
37	eMIOS channel 7 flag	eMIOS channel 7 flag	N/A
38	eMIOS channel 10 flag	eMIOS channel 10 flag	N/A
39	eMIOS channel 11 flag	eMIOS channel 11 flag	N/A
40	eMIOS channel 16 flag	eMIOS channel 16 flag	N/A
41	eMIOS channel 17 flag	eMIOS channel 17 flag	N/A
42	eMIOS channel 18 flag	eMIOS channel 18 flag	N/A
43	eMIOS channel 19 flag	eMIOS channel 19 flag	N/A
44	eTPUA channel 12 data transfer request status	eTPUA channel 12 data transfer request status	N/A
45	eTPUA channel 13 data transfer request status	eTPUA channel 13 data transfer request status	N/A
46	eTPUA channel 28 data transfer request status	eTPUA channel 28 data transfer request status	N/A
47	eTPUA channel 29 data transfer request status	eTPUA channel 29 data transfer request status	N/A
48	SIU external interrupt flag 0	SIU external interrupt flag 0	N/A
49	SIU external interrupt flag 1	SIU external interrupt flag 1	N/A
50	SIU external interrupt flag 2	SIU external interrupt flag 2	N/A
51	SIU external interrupt flag 3	SIU external interrupt flag 3	N/A
52	Decimation filter A fill buffer	eTPUB channel 0 data transfer request status	N/A
53	Decimation filter A fill buffer	eTPUB channel 1 data transfer request status	N/A
54	Decimation filter B fill buffer	eTPUB channel 2 data transfer request status	N/A
55	Decimation filter B fill buffer	eTPUB channel 3 data transfer request status	N/A
56	eSCIC combined DMA request of the Transmit Data Register Empty, Transmit Complete, and LIN Transmit Data Ready DMA requests	eTPUB channel 12 data transfer request status	N/A
57	eSCIC combined DMA request of the Receive Data Register Full and LIN Receive Data Ready DMA requests	eTPUB channel 13 data transfer request status	N/A
58	Reserved	eTPUB channel 14 data transfer request status	N/A
59	Reserved	eTPUB channel 15 data transfer request status	N/A

Table 14. DMA sources for MPC5644a, MPC5566, and MPC5565 (continued)

DMA CH	MPC5644A DMA source description	MPC5566 DMA source description	MPC5565 DMA source description
60	Reserved	eTPUB channel 28 data transfer request status	N/A
61	Reserved	eTPUB channel 29 data transfer request status	N/A
62	Reserved	eTPUB channel 30 data transfer request status	N/A
63	Reserved	eTPUB channel 31 data transfer request status	N/A

One notable difference between MPC5644A and MPC556x devices is that the Nexus DMA data trace module is not implemented on the MPC5644A.

4.1.3.2 eDMA: new features

A new feature that the MPC5644A implements, compared to MPC556x devices, is the minor loop offset. This allows offsets to be applied between minor loops of the eDMA, which is especially useful for transferring several arrays in one major loop. New bit fields have been implemented in the DMA transfer control descriptor (TCD), in the area previously used by the NBYTES field. The new bits that have been implemented are the source minor loop offset enable (SMLOE), the destination minor loop offset enable (DMLOE), and the minor loop offset (MLOFF).

Figure 7 provides an example of how the new minor loop offset feature can be used.

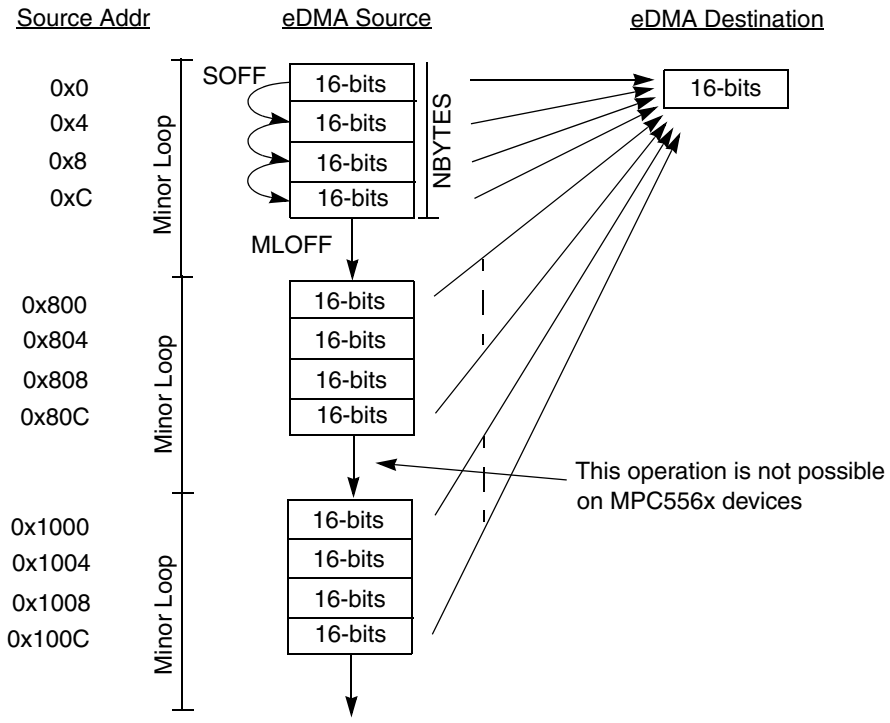


Figure 7. Example of using eDMA minor loop offset feature on MPC5644A

4.1.4 FMPLL

The MPC5644A employs an enhanced FMPLL module that is not completely register-compatible with the FMPLL module used on the MPC556x.

4.1.4.1 FMPLL: software compatibility

While the configuration of the FMPLL on the MPC5644A is similar to that on the MPC556x, the setting controls have been placed in two registers rather than one. Software must be modified to use the new configuration registers. Additionally, due to the change in the crystal frequency range and bit definitions of the dividers in the configuration registers, the desired system frequency must be recalculated using the new algorithm.

The ESYNCR1 and ESYNCR2 are new FMPLL registers used to set the system frequency on the MPC5644A. They are shown in Figure 8 and Figure 9.

Addr: 0xC3F80008 Access: User read/write

R	EMODE	CLKCFG			0	0	0	0	0	0	0	0	EPREDIV			
W																
Reset	0	0	1	–[1]	0	0	0	0	0	0	0	0	1	1	1	1

R	0	0	0	0	0	0	0	0	0	EMFD						
W																
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

1 Reset value determined by the PLLREF pin.

Figure 8. Enhanced Synthesizer Control Register 1 (ESYNCR1)

Addr: 0xC3F8000C Access: User read/write

R	0	0	0	0	0	0	0	0	LOCEN	LOLRE	LOCRE	LOLIRQ	LOCIRQ	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ERFD	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Figure 9. Enhanced Synthesizer Control Register 2 (ESYNCR2)

The relationship between input and output frequency is determined by the EPREDIV, EMFD, and ERFD values programmed in the ESYNCR1 and ESYNCR2 registers, according to Equation 3.

$$f_{sys} = f_{ref} \times \frac{EMFD}{(EPREDIV + 1) \times 2^{(ERFD + 1)}}$$

Eqn. 3

4.1.4.2 FMPLL: new features

The FMPLL includes new ESYNCR1 and ESYNCR2 registers as mentioned above in Section 4.1.4.1, "FMPLL: software compatibility."

4.1.5 Interrupt controller (INTC)

4.1.5.1 INTC: software compatibility

For common features, software written for the MPC556x devices should be compatible with the MPC5644A.

Interrupt vectors from the MPC556x devices have been maintained in the same location on the MPC5644A for compatibility.

4.1.5.2 INTC: new features

The INTC mechanism remains identical — however, the MPC5644A implements 476 request sources to handle new modules and features.

4.1.6 Memory protection unit (MPU)

The MPC5644A provides a new memory protection module (MPU).

4.1.6.1 MPU: software compatibility

The MPU is a new module implemented on the MPC5644A. By default, the MPU is not enabled and requires no changes to existing code.

4.1.6.2 MPU: new features

The MPU provides hardware access control for all memory references generated in a device. Using 16 preprogrammed region descriptors that define memory spaces and their associated access rights, the MPU concurrently monitors all system bus transactions and evaluates the appropriateness of each transfer. Memory references with sufficient access control rights are allowed to complete; references that are not mapped to any region descriptor or have insufficient rights are terminated with a protection error response.

4.1.7 System integration unit (SIU)

The SIU on the MPC5644A is largely compatible with the SIU on the MPC556x devices.

4.1.7.1 SIU: software compatibility

Where possible, Pad Configuration Register numbering has been kept compatible between the MPC5644A and MPC556x. Existing code may have to be modified to incorporate different pin multiplexing functions within the SIU Pad Configuration Registers (PCR).

Only fourteen external interrupt requests are implemented on the MPC5644A.

MPC5644A supported external IRQs:

- IRQ[0:5]
- IRQ[7:15]

MPC5644A unsupported external IRQ:

- IRQ[6]

Any software for the MPC556x that utilizes external IRQ[6] will need to be modified.

A clock divider for the FlexCAN has been included in the SIU. If you intend to run the system frequency at greater than 100 MHz, then this clock divider must be configured to ensure correct CAN operation. More information is provided in Section 4.1.7.2, "SIU: new features."

New multiplexing has been introduced for the input of eTPUA[24:29], via the SIU_ISEL8 register. This allows the inputs for these eTPU channels to originate from a DSPI deserialized output or the respective ball on the device package. This register bypasses any settings in the respective SIU_PCR register. This configuration is shown in Figure 10.

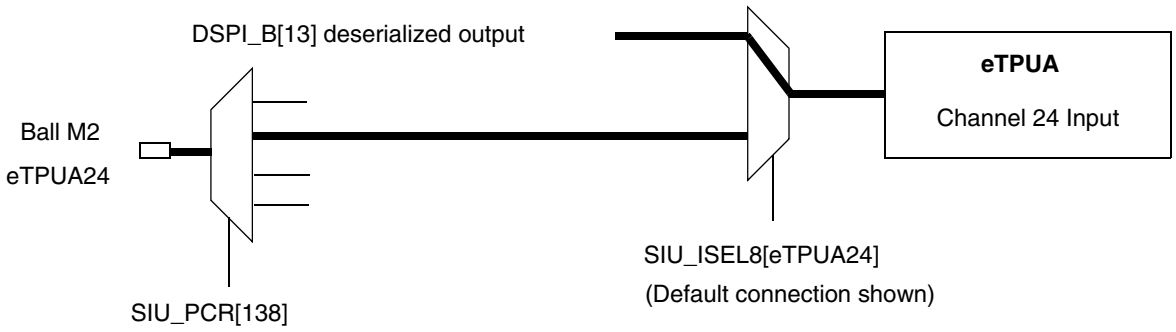


Figure 10. MPC5644A SIU multiplexing for eTPUA24

By default, the inputs for eTPUA[24:29] will originate from the DSPI deserialized output, and not the respective package ball.

Any software that relies on the inputs for eTPUA[24:29] originating from the external ball will need to modify the values in the SIU_ISEL8 register.

4.1.7.2 SIU: new features

- A new MUX Select 3 register (SIU_ISEL3) has been implemented to extend the eQADC trigger sources. Using a combination of the SIU_ETISR and the SIU_ISEL3 registers, the eQADC can now be triggered from the PIT, RTI, and an additional eTPU channel.
- An additional MCU Identification Register (SIU_MIDR2) is implemented to provide additional information about the MCU.
- New sources of reset have been added to the SIU Reset Status Register (SIU_RSR) for the SWT.
- SIU Halt and Halt Acknowledge registers have been implemented to support the low power modes detailed in Section 4.2.5, "Low power modes."
- Additional PCRs have been included to support DSPI serialization. The source for the DSPI serialization can be taken from PCR[350:413]. These can be thought of as "virtual" PCRs as they are not connected to any external pins. Each bit of the DSPI serialization data refers to one unique PCR, in which the appropriate eMIOS, eTPU, or GPIO source can be selected.
- A new clock divider for the FlexCAN has been included in the SIU registers. The FlexCAN module is derived from this clock when the CAN_CR[CLK_SRC] bit is set to one (Bus Clock selected).

The FlexCAN module is limited to a 100 MHz clock; therefore, this register must be set to one (to divide the system frequency) for system frequencies of over 100 MHz.

Figure 11 details the SYSDIV register in the SIU from where this clock divider is set. The CAN is to be derived directly from the system clock. If you intend to run a system frequency of greater than 100 MHz, this register must be appropriately configured.

SIU + 0x09A0 — Access: User read/write

	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CAN 2:1
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	0	0	0	0	0	0	0	0	0	0	0					
R	0	0	0	0	0	0	0	0	0	0	0	BY PASS	SYSCLKDIV		0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 11. SIU_SYSDIV

Table 15. SIU_SYSDIV register description

Field	Description
CAN2:1	0 When CAN_CR[CLK_SRC]=1, FlexCAN runs at the system frequency 1 When CAN_CR[CLK_SRC]=1, FlexCAN runs at half the system frequency
BYPASS	Bypass bit 0 System clock divider is not bypassed 1 System clock divider is bypassed
SYSCLKDIV	System Clock Divide The SYSCLKDIV bits select the divider value for the system clock (ipg_clk). Note that the SYSCLKDIV divider is required in addition to the RFD to allow the other sources for the system clock (16 MHz IRC and OSC) to be divided down to slowest frequencies, to improve power. The output of the clock divider is nominally a 50% duty cycle. 00 Divide by 2 01 Divide by 4 10 Divide by 8 11 Divide by 16

4.1.8 Watchdog (WDT/SWT)

The MPC5644A implements two separate watchdogs, one within the e200z4 core (WDT) and one in a dedicated software watchdog timer (SWT) module. The SWT is mainly intended for AutoSAR applications.

4.1.8.1 WDT: software compatibility

Software written for the e200z6 watchdog will be compatible with the e200z4 watchdog. It may, however, need modification to adjust timeout values, due to the different operating frequencies of the MPC5644A.

4.1.8.2 SWT: new features

A new software watchdog, located on the peripheral bridge, has been included in the MPC5644A. The software watchdog timer (SWT) has the following features:

- 32-bit timeout register to set the timeout period
- Programmable selection of system or oscillator clock for timer operation
- Programmable selection of window mode or regular servicing
- Programmable selection of reset or interrupt on an initial timeout
- Programmable selection of fixed or keyed servicing
- Master access protection
- Hard and soft configuration lock bits

At startup, the BAM can enable either the core watchdog or the SWT using the reset configuration halfword (RCHW). Debuggers do not normally run the BAM, so debuggers must also disable the SWT. If not disabled by the RCHW and booting from flash memory, software must disable the SWT early in the initialization sequence.

4.1.9 Crossbar (XBAR)

The MPC5644A uses the same crossbar mechanism as the MPC556x devices.

4.1.9.1 XBAR: software compatibility

The master and slave ports for these devices are shown in Table 16 below.

Table 16. XBAR switch ports

	XBAR port (master/slave)	MPC5565	MPC5566	MPC5644A
e200z6 core — CPU instruction/data e200z4 core — CPU instruction	Master 0	Valid	Valid	Valid
e200z6 — Nexus				n/a
eDMA	Master 1	Valid	Valid	Valid
External bus interface	Master 2	Valid	Valid	Valid
Fast Ethernet controller	Master 3	Reserved	Valid	n/a
e200z4 — CPU data	Master 4	n/a	n/a	Valid
e200z4 — Nexus		n/a	n/a	
FlexRay	Master 6	Reserved	n/a	Valid
Flash memory	Slave 0	Valid	Valid	Valid
External bus interface	Slave 1	Valid	Valid	Valid
Internal SRAM	Slave 3	Valid	Valid	Valid
Peripheral bridge A (PBRIDGE_A)	Slave 6	Valid	Valid	n/a
Peripheral bridge B (PBRIDGE_B)	Slave 7	Valid	Valid	Valid

The setting of the XBAR Master Priority Register (XBAR_MPRx) for each slave needs to be considered when migrating to the MPC5644A. Each master must be assigned a unique priority in this register; therefore, any existing software written for the MPC556x XBAR_MPRx should be modified to comply with this requirement.

Existing software written for the MPC556x devices does not modify these registers when the default values are used. This approach can also be used for the MPC5644A.

The Harvard architecture used on the MPC5644A brings new considerations for the XBAR_MPRx settings. By default, the CPU instruction master has highest priority to the flash memory. There is a potential condition in which the CPU instruction master can dominate the accesses to the flash memory and restrict access of other masters. It is recommended that the settings in Table 17 be used to get the optimal performance from the XBAR.

Table 17. Recommended XBAR_MPR*x* settings

Slave	MSTR_0 (CPU Instruction)	MSTR_1 (DMA)	MSTR_2 (EBI)	MSTR_4 (CPU Data)	MSTR_6 (FlexRay)
Default [1]	0x0	0x1	0x2	0x3	0x4
Internal flash	0x4	0x0	0x1	0x2	0x3
Internal SRAM	0x4	0x1	0x2	0x3	0x0[2]
Peripheral bridge	0x4	0x1	0x2	0x3	0x0

1 Default settings applied to each XBAR_MPRx register.

2 FlexRay is given highest priority for instant access to message buffers.

4.1.9.2 XBAR: new features

New masters are present on the MPC5644A: the e200z4 data master (due to Harvard architecture) and FlexRay master as described above.

4.2 e200z4 Core

The MPC5644A implements an e200z4 core. The key differences between the e200z4 and the e200z6, which is implemented on MPC556x devices, are shown in Table 18.

Table 18. e200z4 vs e200z6 Differences

Feature	MPC556x e200z6	MPC5644A e200z4	Software considerations
Pipeline	Single issue 7 Stage	Dual issue 5 Stage	Dual issue optimized compiler is recommended for maximum e200z4 performance
Bus structure	Unified 64-bit	Harvard 64-bit	Additional XBAR settings required
Instruction set	VLE BookE	VLE BookE	None
Cache	8/32KB Unified	8KB Instruction only	Cache initialization registers are different
Branch target buffer	8 Entry	8 Entry	Different configuration registers
Signal processing engine (SPE)	SPE 1.1	SPE 1.1	None
Memory management unit (MMU)	32 Entry	16 Entry	Fewer memory mapped regions will be available — software may have to be modified to reflect this
Interrupts and exceptions	IVOR0–15 IVOR32–34 SSR0/1 CSSR0/1 DSSR0/1	IVOR0-15 IVOR32-34 SSR0/1 CSSR0/1 DSSR0/1 MSSR0/1 Non maskable interrupt(NMI) New context save/restore instructions	New Machine Check Save/Restore Register — IVOR1 handler would need to be updated to support this change External NMI pin can be used for IVOR1 exceptions Interrupt handler efficiency can be improved using new context save/restore instructions

4.2.1 Cache

The MPC5644A uses an 8 KB instruction cache, compared to the unified cache architecture that is used on the MPC556x devices. The initialization of the instruction cache uses the same procedure as the unified cache; however, it utilizes a new register, the L1CSR1.

4.2.1.1 Cache: software compatibility

The MPC556x devices use the L1 Cache Control and Status Register 0 (L1CSR0) to configure the cache. These register contents are shown in Figure 12.

The MPC5644A uses two registers for its cache initialization, the L1CSR0 and the L1 Cache Control and Status Register 1 (L1CSR1). The contents of these registers are shown in Figure 13 and Figure 14.

The L1CSR1 register is specifically implemented due to the Harvard architecture bus and instruction cache support. Many of the bit fields in the L1CSR1 register mirror the operation of the respective fields in the MPC556x L1CSR0 register.

The L1 Cache Configuration Registers (L1CFG0 and L1CFG1) can be used by software to determine the type of cache being used (unified/Harvard) and the size of the cache available. Further details of the L1CSR1, L1CFG0, and L1CFG1 registers can be found in the e200z4 core reference manual.

4.2.1.1.1 Cache initialization

The recommended cache initialization sequence for the MPC5644A is as follows:

1. Ensure that any prior invalidation of the cache is completed.
   - Check L1CSR1[ICABT]. If set, poll this bit until complete.
2. Invalidate the cache by setting L1SCSR1[ICINV]=1.
   - Reset does not invalidate the cache automatically.
3. Once set, hardware clears L1CSR1[ICINV] after the cache has been invalidated.
   - During this time, CPU waits for cache invalidation to complete. Code is not executed.
   - Software should poll L1CSR1[ICINV] bit to ensure it is cleared.
   - Software should also poll L1CSR1[ICABT] to check for a cache abort.
4. Execute msync and isync instructions.
5. Enable cache by setting L1CSR1[ICE]=1.
6. In the MMU, the TLB[I] (Cache Inhibited) bit must be cleared for memory areas that are to be cached.

4.2.1.2 Cache: new features

4.2.1.2.1 Cache error detection and automatic correction

The MPC556x devices have parity checking on the cache tags and data. Any parity error that could result in incorrect operation will cause a machine check exception. The MPC5644A also supports this mechanism, but it has an additional new feature that can automatically handle cache errors in hardware: error detection code (EDC) protection.

The hardware for EDC protection allows single-bit tag errors in the cache to be corrected automatically. If a multi-bit error or data error in the cache line is detected, the hardware can also automatically invalidate the cache line and refill it from memory, without generating an exception.

The cache error-handling mechanisms can be tested by injecting errors into the cache using the L1CSR[ICEI] bit shown below.

Table 19. MPC5644A L1CSR1 cache error injection bit descriptions

Bits	Name	Description
16	ICEI	Instruction Cache Error Injection Enable 0 Cache error injection is disabled. 1 When ICEDT = 00, parity errors will be purposefully injected into every byte subsequently written into cache. The parity bit of each 8-bit data element written will be inverted on cache linefills. When ICED = 01, a double-bit error will be injected into each doubleword written into the cache by inverting the two uppermost parity check bits. ICEI will cause injection errors regardless of the setting of ICECE, although reporting of errors will be masked when ICECE = 0.

4.2.2 Branch target buffer

4.2.2.1 Branch target buffer: software compatibility

On the e200z6 core, the branch target buffer (BTB) is configured using two different registers: the HID0[BPRED] bit field and the BUCSR register.

On the e200z4, the functionality of the HID0[BPRED] bit field has been removed from the HID0 register and integrated into the BUCSR register. Software will need to be modified to reflect this change.

4.2.2.2 Branch target buffer: new features

The allocation of branch target buffer entries on the e200z4 may be controlled using the BUCSR[BALLOC] field to control whether forward or backward branches (or both) are candidates for entry into the BTB, and thus for branch prediction.

4.2.3 Instruction set

The variable-length encoding (VLE) and BookE instruction sets are supported by both MPC556x and MPC5644A processors.

4.2.3.1 Instruction set: software compatibility

The instruction sets are software compatible between the MPC556x devices and the MPC5644A.

4.2.3.2 Instruction set: new features

New VLE instructions have been added to the MPC5644A which allow more efficient context save and restore routines. These are described in more detail in section Section 4.2.4.2.1, “New interrupt save/restore instructions.”

To get the maximum performance out of the e200z4 core on the MPC5644A, a compiler that schedules instructions optimally for a dual issue pipeline is recommended.

4.2.3.3 Memory management unit (MMU)

The e200z4 core implements fewer MMU TLB entries than the e200z6 core, twenty-four entries compared to thirty-two entries.

4.2.3.4 MMU: software compatibility

If software written for the MPC556x device utilizes the upper twenty-four MMU entries, then these accesses will have to be removed for compatibility with the MPC5644A device.

4.2.3.5 MMU: new features

To supplement the MMU, a memory protection unit (MPU) is included in the MPC5644A. This allows the user to assign up to sixteen memory regions with different access privileges. Unlike the MMU, the MPU is used to monitor bus accesses from all masters. More information can be found in Section 4.1.6, "Memory protection unit (MPU)."

The MMU implements a new feature which allows MMU mapping to be switched using an external tool with no modification to software. This feature is specifically intended for calibration tools which need to dynamically re-map calibration data from internal flash memory to external RAM.

4.2.4 Interrupts and exceptions

The majority of interrupt and exception functionality that is available on the MPC556x is compatible with the MPC5644A.

4.2.4.1 Interrupts and exceptions: software compatibility

The handling of a machine check (IVOR1) exception is different on the MPC5644A due to the implementation of new machine check save and restore registers. These are detailed in Section 4.2.4.2.3, "Machine check save/restore registers." If the MPC556x IVOR1 interrupt handler does not return the core back to the program flow (for example, due to a non-recoverable exception) then this will not impact its operation and existing code can be re-used.

With the exception of this situation, existing code can be re-run without any modifications.

4.2.4.2 Interrupts and exceptions: new features

New features that have been implemented on the MPC5644A are:

- New interrupt save/restore instructions
- Non-maskable interrupt (NMI)
- Machine Check Save/Restore registers

4.2.4.2.1 New interrupt save/restore instructions

The most significant of these enhancements are the new VLE instructions which enable more efficient interrupt handling.

The new instructions allow the user to save and restore register context in single instructions. The e200z4 registers are split into four groups:

- Volatile General Purpose registers: R0, R3:R12
- Volatile Special Purpose registers: CR, LR, XER, and CTR
- Volatile Save and Restore register: SRR0/1
- Volatile Critical Save and Restore register: CSRR0 and CSRR1
- Volatile Debug Save and Restore register: DSRR0 and DSRR1

Using the new instructions, each of these groups can be stored or loaded in a single instruction.

These new instructions will improve the latency of the interrupt handler as they will perform 64-bit bus accesses when storing/loading registers, compared to the 32-bit accesses with single store/load instructions. The instructions will also reduce interrupt handler code space, which may be more significant if operating interrupts in hardware vector mode.

More detailed information can be found in Freescale document EB696, *New VLE Instructions for Improving Interrupt Handler Efficiency*, available at www.freescale.com.

4.2.4.2.2 Non-maskable interrupt (NMI)

The MPC5644A has the inclusion of a non-maskable interrupt (NMI) pin. The WKPCFG_NMI_GPIO[213] pin has the NMI functionality multiplexed on it. To use the NMI there are several registers which need to be set up:

1. Configure the NMI functionality on the WKPCFG pin. This is achieved via the SIU_PCR213 register. The PA field must be set to the NMI functionality (SIU_PCR213[PA] = 0b0010), and the input buffer enabled (SIU_PCR213[IBE] = 0b1). The internal weak pulls can optionally be used to pull the signal to a default level.
2. Configure External IRQ registers within the SIU module to enable NMI functionality and set up which exception is started when the NMI signal is triggered.

The SIU External IRQ Rising/Falling-Edge Event Enable registers (SIU_IREER and SIU_IFEER) enable an NMI event for a rising edge or falling edge respectively. By default, both of these are disabled, so to enable NMI events, one or both of these registers must be programmed accordingly.

The SIU DMA/Interrupt Request Enable register (SIU_DIRER) selects which e200z4 core exception will be started on an NMI event. By default, the SIU_DIRER[NMI_SEL] bit is set to 0. This results in a machine check exception (IVOR1) if an NMI event occurs. If the SIU_DIRER[NMI_SEL] is set to 1, then a critical exception (IVOR0) will occur on an NMI event.

4.2.4.2.3 Machine check save/restore registers

The e200z4 core on the MPC5644A implements new Machine Check Save and Restore registers (MCSRR0 and MCSRR1). These have the same functionality as the Save and Restore registers (SRR0/1), however will be used whenever a machine check exception occurs.

A new instruction, the return from machine check interrupt (RFMCI) has also been implemented to return from an IVOR1 exception using the contents of MCSRR0 and MCSRR1.

4.2.5 Low power modes

The MPC5644A implements some power-saving techniques to reduce battery usage when the engine is switched off.

4.2.5.1 Low power modes: software compatibility

The low power modes are new on the MPC5644A. By default, the low power modes are not enabled and require no changes to existing code.

4.2.5.2 Low power modes: new features

It is possible to gate clocks to modules on the MPC5644A using the SIU Halt registers (SIU_HLT). The e200z4 can also be halted upon execution of a wait instruction. The CPU can be woken from this halted state upon reception of any interrupt request.

There are two defined low power modes for the MPC5644A: slow mode and stop mode. To enter these modes the user has to set up multiple configuration settings (including FMPLL, SIU_HLT, and wait instruction) as per the descriptions below.

Slow mode is defined as follows:

- FMPLL running in bypass mode
- System clock set to 1 MHz (using system clock divider)
- PLL shut down
- CPU running simple executive code
- 4 × ADC conversion every 10 ms
- 2 × PWM channels at 1 kHz
- All other modules stopped via SIU_HLT register

Stop mode is defined as follows:

- FMPLL running in bypass mode
- System clock set to 1 MHz (using system clock divider)
- CPU stopped (using wait instruction)
- PIT running
- All other modules stopped via SIU_HLT register

4.3 Internal/external memory

4.3.1 Flash

The MPC5644A has 4 MB of flash memory, increased from the 2 MB and 3 MB of flash memory on the MPC5565 and MPC5566, respectively.

4.3.1.1 Flash: software compatibility

- The MPC5644A requires a different flash memory programming algorithm that will be provided by Freescale as a software driver. Any proprietary flash memory programming algorithms or drivers must be re-coded for the MPC5644A.
- Any PC tools used for programming flash memory will need to be updated.
- There are now two sets of control registers, one for each flash array.
- The flash memory block sizes have changed as shown in Table 20.

Table 20. MPC5566 vs MPC5644A flash partitions

MPC5566	
Array (256-bit)	
Block size	Use
2 × 16K 2 × 48K 2 × 64K	Low address space
2 × 128K	Mid address space
20[1] × 128K	High address space

MPC5644A			
Array A (128-bit)		Array B (128-bit)	
Block size	Use	Block size	Use
8 × 16K 2 × 64K	Low address space		
2 × 128K	Mid address space		
		256K	Low address space
		256K	Mid address space
6 × 256K	High address space	6 × 256K	High address space

[1] 12 × 128K on MPC5565

4.3.1.2 Flash: new features

The MPC5644A ECC supports single-bit error reporting for flash memory.

4.3.2 SRAM

There is 192 KB of SRAM implemented on the MPC5644A, including 32 KB which have standby supply functionality.

4.3.2.1 SRAM: software compatibility

The size of the SRAM has increased compared to the MPC556x devices, which implements SRAM sizes of 64 KB, 80 KB, and 128 KB. Initialization software will have to be modified to initialize the error correction codes (ECC) in the new RAM locations of the MPC5644A.

The location of standby RAM is compatible between MPC5644A and MPC556x devices.

4.3.2.2 SRAM: new features

The SRAM supports user-configurable read wait states, with options of zero or one wait state. To operate at maximum specified system frequency, one wait state will be required. At reduced system frequencies, the device will be able to operate with a zero wait state. Please refer to the MPC5644A data sheet for details on the frequency requirements for one wait state.

The SRAM read wait state can be set in the miscellaneous control module (MCM) MUDCR register. The register is based at the following location: ECSM base + 0x24, (0xFFF4_0024). Figure 12 details this register.

ECSM + 0x0024 — Access: User read/write

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	PWSC	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 12. Miscellaneous User-Defined Control Register (MUDCR)

Table 21. MUDCR register description

Field	Description
PWSC	SRAM Wait State Control 0 SRAM is set to zero read wait states 1 SRAM is set to one read wait state

4.3.3 External bus interface (EBI)

4.3.3.1 EBI: compatibility

There is a high level of compatibility between the MPC556x and the MPC5644A for the external bus interface, both from a hardware and software perspective. However, there are differences and new features which must be considered when using the MPC5644A EBI.

Table 22 and Table 23 detail the EBI configurations that are available on the MPC5644A. It is shown that there is a signal-compatible 16-bit non-multiplexed mode to the MPC556x; however, there are frequency limitations on the maximum operating frequency as medium speed pads are used in this configuration (compared to fast pads on the MPC556x).

Table 22. MPC556x vs MPC5644A EBI configuration options

	MPC556X	MPC5644A		
Configuration	16-bit non-multiplexed	16-bit non-multiplexed	16-bit multiplexed	32-bit multiplexed
Maximum operating frequency	$f_{SYS}/2$	$f_{SYS}/4$	$f_{SYS}/2$	$f_{SYS}/4$

Table 23. MPC556x vs MPC5644A EBI Signals

Memory connection[1]	MPC556X Signal	MPC5644A Signal[2,3]		
	16-bit non-multiplexed	16-bit non-multiplexed[4]	16-bit multiplexed[5,6]	32-bit multiplexed[6,7]
ADDR[12:15]	ADDR[12:15]	ADDR[12:15]	ADDR[12:15]	DATA[12:15][8]
ADDR[16:31]	ADDR[16:31]	ADDR[16:31]	DATA[0:15]	ADDR[16:31]
DATA[0:15]	DATA[0:15]	DATA[0:15]	DATA[0:15]	DATA[0:15]
DATA[16:31]	N/A	N/A	N/A	ADDR[16:31]
WE[0:1]	WE[0:1]	WE[0:1]	WE[0:1]	WE[0:1]
WE[2:3]	N/A	N/A	N/A	ADDR[13:14][9]
TS	TS	TS	TA[10]	TA[10]
ALE	N/A	N/A	TS[11]	TS[11]

1 Only signals which have alternative settings are listed here. Signals not mentioned here, such as CS, OE, and RD_WR, can be assumed to have compatible signal naming.

2 On the DATA[0:15] signals, it is possible to multiplex the ADDR[16:31] signals by setting the EBI_BRx[AD_MUX] bit.

3 On the ADDR[16:31] signals, it is possible to multiplex the DATA[16:31] signals by setting the EBI_BRx[AD_MUX] bit, and by selecting Alternate 2 functionality on the PCR[PA] field.

4 In the EBI the following bits are configured: EBI_BRx[AD_MUX] = 0, EBI_BRx[PS] = 1.

5 In the EBI the following bits are configured: EBI_BRx[AD_MUX] = 1, EBI_BRx[PS] = 1, and EBI_MCR[D16_31] = 0. The PCR[PA] settings for DATA[0:15] are set to Primary functionality.

6 Typically, an external latch is used to de-multiplex the bus using the ALE signal. Some synchronous memories can de-multiplex the EBI without the need for an external latch. Please refer to the specific memory's data sheet.

7 In the EBI the following bits are configured: EBI_BRx[AD_MUX] = 1, EBI_BRx[PS] = 0. The PCR[PA] settings for ADDR[16:31] are set to Alternate 2 functionality (DATAxx).

[8] For smaller memories, the ADDR[15] signal could be used. However, ADDR[13:14] are required for extending the Write/Byte enable signal for 32-bits.

[9] The PCR[PA] for ADDR[13:14] are set to Alternate 2 functionality (WE[2:3]).

[10] The PCR[PA] for TA is set to Alternate 1 functionality (TS).

[11] The PCR[PA] for TS is set to Alternate 1 functionality (ALE).

4.3.3.2 EBI: new features

The multiplexed bus feature has been implemented on the MPC5644A. Table 22 and Table 23 show the configurations that are available for the multiplexed bus.

To de-multiplex the bus signals at the memory, there are two approaches that can be used.

- The first method is to use an external latch that latches the address pins on the assertion of the ALE signal. A device such as the 74LVC16373A could be used for this purpose.
- The other approach is to rely on the memory to de-multiplex the address signals during the first clock cycle phase. This method depends on the memory device being used (the memory data sheet would have to be consulted). However, synchronous memories are typically suited to this operation.

New bit fields have been introduced into the EBI_MCR and EBI_BRx registers to enable and configure the multiplexed bus. The key bit fields for chip select mapped registers are:

- EBI_MCR[D16_31] — Controls whether the EBI uses the DATA[0:15] or DATA[16:31] signals for the 16-bit bus when in 16-bit multiplex mode.
- EBI_BRx[AD_MUX] — Enables multiplexed mode.

4.3.4 Calibration bus interface (CAL_EBI)

4.3.4.1 CAL_EBI: compatibility

The MPC5644A calibration bus is compatible with the MPC556x calibration bus from a hardware perspective. Modifications will have to be made to software as the Pad Configuration registers (PCR) for the calibration bus signals differ between the two devices. These differences are highlighted in Table 24.

Table 24. Calibration bus interface PCR differences

Calibration bus signal	MPC556x PCR#	MPC5644A PCR#
CAL_CS0	256	336
CAL_CS2	257	338
CAL_CS3	258	339
CAL_ADDR[12:15]	259:262	340
CAL_ADDR[16:30]	263:277	345
CAL_DATA[0:15]	278:293	341
CAL_RD_WR	294	342

Table 24. Calibration bus interface PCR differences (continued)

Calibration bus signal	MPC556x PCR#	MPC5644A PCR#
CAL_WE0	295	342
CAL_WE1	296	342
CAL_OE	297	342
CAL_TS	298	343

4.3.4.2 CAL_EBI: new features

The calibration bus on the MPC5644A supports two new features:

- Burst accesses to synchronous memories. This is available via the CAL_BDIP signal.
- A 32-bit multiplexed bus, similar to the EBI implementation.

4.4 Analog

4.4.1 Enhanced queued analog-to-digital converter (eQADC)

4.4.1.1 eQADC: software compatibility

For common features, software written for the MPC556x devices should be compatible with the MPC5644A.

4.4.1.2 eQADC: new features

There have been several new features introduced on the MPC5644A eQADC. By default, these features are disabled, or in a state that is backwardly compatible with the MPC556x.

Wider range of trigger inputs

- A wider range of trigger inputs is now available, including PIT timers, and eTPU AND'ed with PIT timers. There is a new register in the SIU (SIU_ISEL3) that allows a wider selection of trigger inputs. By default, the trigger selection in the SIU is backwardly compatible with software written for the MPC556x.

Additional eQADC input channels

- It is possible to monitor more internal signals using eQADC channels on the MPC5644A. Power domains and bandgap voltages from the power management controller (PMC) can now be monitored by ADC conversions. There is also the inclusion of an on-chip temperature sensor, which can be monitored via an eQADC channel.

Variable gain amplifier (VGA)

- A variable pre-gain stage is introduced with the VGA. This allows users to amplify a differential input by ×1, ×2 or ×4 at the input stage (in other words before the ADC) of a differential channel. The benefit of this is improved resolution for small differential voltages.

Configurable weak pulls on differential channels

- Configurable weak pulls have been implemented on differential channels to allow sensor biasing and provide a new mechanism for sensor diagnostics. Each differential channel can be configured independently to operate with either weak pullup, weak pulldown, center bias, or no bias. The weak pull values are also independently configurable between 200 kΩ, 100 kΩ, and 5 kΩ.

Command queue (CQUEUE) streaming

- On the MPC556x eQADC, once a command had been passed from the CFIFO to the ADC to perform a conversion, the command is invalidated in the CFIFO. For small command queues, where only a couple of commands are ever used, this means that the eDMA or core would have to continually transfer the same commands to the CFIFO, once the previous commands were invalidated.
- On the MPC5644A, a streaming feature has been implemented to bypass this situation. This feature allows you to choose whether commands in the CFIFO are invalidated after they have been passed to the ADC for conversion. This feature is only implemented on CFIFO0, but, once enabled,

extends the CFIFO0 size to eight entries. This allows up to eight commands to be stored in CFIFO0, and it allows for the continuous conversion of these commands without their having to be updated by the eDMA or core.

Abort feature

- The abort feature allows you to send a high priority conversion command that will bypass the internal ADC buffers and immediately abort the current conversion (which is restarted after the high priority conversion), thereby allowing the ADC to convert the high priority command.

Decimation filter

- A configurable decimation filter has been implemented on the MPC5644A. This provides a mechanism to directly filter eQADC results before they are transferred to the RFIFO. The decimation filter implements up to a 4th-order IIR filter or 8th-order FIR filter, as shown in Figure 13 below. It also includes 24-bit programmable coefficients and a 51-bit accumulator.
- It is possible to use the decimation filter in two ways.
  - Independently, whereby the core or eDMA can pass data into the filter, and the result is transferred back out via the same mechanism.
  - Integrated with the eQADC, whereby ADC results are transferred via the decimation filter, and the output from the filter is transferred into the appropriate RFIFO on the eQADC. This way, the decimation filter is transparent to software.

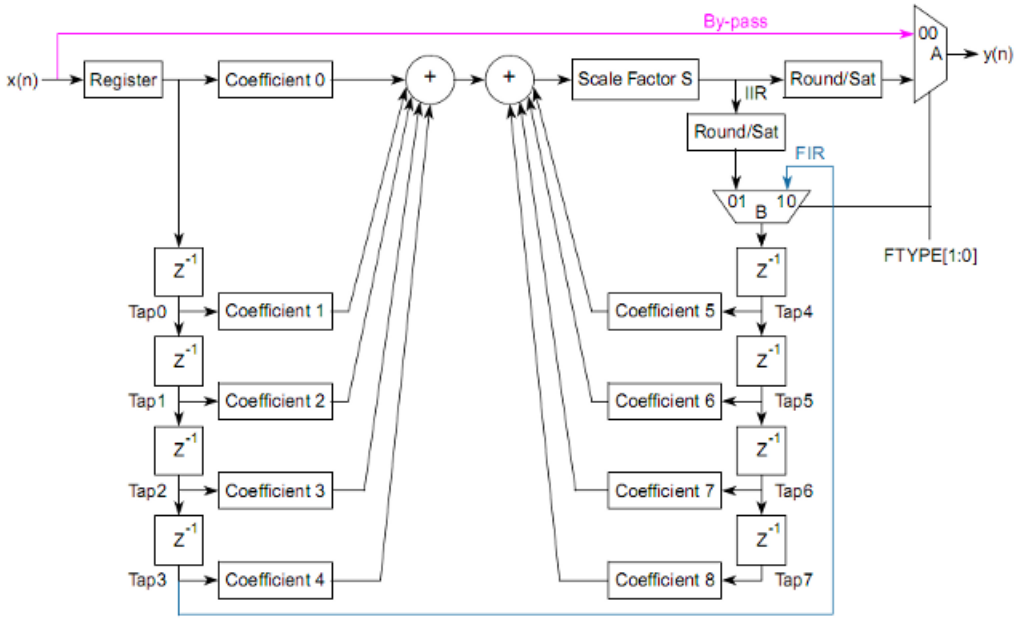


Figure 13. Decimation filter configuration

eQADC timebase from STAC bus

- It is possible to select one of the eTPU timebases from the STAC bus, as the time-stamping source in the eQADC. This allows eQADC results to be time-stamped relative to an angle domain, which can be useful for several engine control applications.

4.5 Timer modules

4.5.1 Configurable enhanced modular IO subsystem (eMIOS)

4.5.1.1 eMIOS: software compatibility

Software written for common unified channel modes between the MPC556x devices will be compatible with the MPC5644A.

The MPC5644A supports fewer unified channel modes than the MPC556x devices. It does not support the non-buffered modes, where buffered alternates are available (namely MC, OPWFM, OPWMC, and OPWM). It also does not support the OPWMCB, PEA, PEC, and QDEC unified channel modes.

4.5.1.2 eMIOS: new features

No new features have been implemented.

4.5.2 Enhanced timed processing unit (eTPU)

4.5.2.1 eTPU: software compatibility

For common features, software written for the MPC556x devices should be compatible with the MPC5644A.

The eTPU code memory size is 14 KB on the MPC5644A — this is different from the MPC556x devices.

4.5.2.2 eTPU: new features

The MPC5644A implements the eTPU2 module. This is backwardly compatible with the eTPU used on the MPC556x devices.

The eTPU2 implements new features such as a watchdog, priority passing, and engine relative addressing. More information on the eTPU2 features can be obtained from Freescale document ETPURMAD, *eTPU Reference Manual Addendum*.

4.5.3 Reaction module

4.5.3.1 Reaction module: software compatibility

The reaction module is a new module implemented on the MPC5644A. By default, the functions of this module are disabled and require no changes to existing code.

4.5.3.2 Reaction module: new features

The reaction module provides closed-loop current control using integrated hardware. The module is highly flexible and can be used for controlling and creating various current waveforms. Applications of this

module range from simple solenoid control in transmission applications to the generation of complex current waveforms for direct injection.

4.5.4 System timer module and periodic interrupt timer (STM/PIT)

4.5.4.1 STM/PIT: software compatibility

The STM and PIT are new modules implemented on the MPC5644A. By default, these timers are not enabled and require no changes to existing code.

4.5.4.2 STM/PIT: new features

Features that the PIT implements:

- 32-bit counter
- Four timer channels
- One real-time interrupt

Features that the STM implements:

- One 32-bit counter with an 8-bit prescaler
- Four 32-bit compare registers

4.6 Communication peripherals

4.6.1 Deserial serial peripheral interface (DSPI)

4.6.1.1 DSPI: software compatibility

For common features, software written for the MPC556x devices should be compatible with the MPC5644A.

4.6.1.2 DSPI: new features

The DSPI has implemented new features to support the microsecond bus protocol. Using selectable timer inputs from the SIU (Section 4.1.7.2, “SIU: new features”) and low voltage differential signals (LVDS), the DSPI can transmit a 32-bit serial data frame to an external ASIC at intended frequencies of up to 40 MHz.

Another new feature of the DSPI module on the MPC5644A is the ability to generate and check parity in a serial frame. More details can be found in Freescale document MPC5644ARM, *MPC5644A Microcontroller Reference Manual*.

4.6.2 Enhanced serial communications interface (eSCI)

4.6.2.1 eSCI: software compatibility

For common features, software written for the MPC556x devices should be compatible with the MPC5644A.

4.6.2.2 eSCI: new features

The eSCI is largely unaltered between the MPC556x and MPC5644A. Some new features that have been added are:

- Inverted polarity for the RXD pin: eSCI_CR2[RXPOL]
- Parity bit masking: eSCI_CR2[PMSK]
- Receive error indication for LIN frames: eSCI_DR[ERR]
- Unrequested data reception interrupt for LIN frames: eSCI_SR[UREQ]

4.6.3 FlexCAN

4.6.3.1 FlexCAN: software compatibility

The FlexCAN module has not been updated with new features. However, the clock providing the FlexCAN block has been implemented differently.

Therefore, software written for the MPC556x devices will be compatible with the MPC5644A, as long as adjustments are made to the FlexCAN clock in the SIU. Please refer to Section 4.1.7.2, “SIU: new features” for more details.

4.6.3.2 FlexCAN: new features

The following new features have been implemented on the FlexCAN.

- Full-featured Rx FIFO
  - Storage capacity for six frames and internal pointer managing
  - Powerful Rx FIFO ID filtering, capable of matching incoming IDs against eight extended, sixteen standard, or thirty-two partial (eight bits) IDs, with individual masking capability
- Additional local priority programmable transmission on individual Tx message buffers
- Hardware cancellation on Tx message buffers

4.7 Nexus and JTAG (debug)

4.7.1 Debug: compatibility

The Nexus and JTAG blocks implemented on the MPC5644A are largely compatible with the MPC556x implementation. From a software perspective, the only notable change is in the Nexus Device ID register (DID) which has a unique entry for the MPC5644A.

The hardware implementation of the JTAG signals is similar between both devices. The same set of signals are used, but the signals use different pad types.

On the MPC556x, the JTAG module is powered by a 3.3 V supply and drives 3.3 V signal levels.

On the MPC5644A, the JTAG module is powered by a 5 V supply; however, the pads drive at a 3.3 V signal level due to the special multivoltage pad type used for the JTAG signals. The multivoltage (MultiV) pads are powered by 5 V but drive at 3.3 V, thereby allowing 3.3 V input/output operation.

More information on the supply configuration is covered in Section 3.5.1.5, "Nexus and JTAG supply."

The hardware implementation of the Nexus signals does vary between the two devices. The same set of signals are used, but they operate in two different configurations. These are shown in Table 25.

Table 25. MPC5644A Nexus configurations

Nexus width	MDO[0:3]	MDO[4:11]	Max freq
Reduced port mode[1]	Nexus data out 0:3	GPIO	f_{SYS} / 2[2, 4]
Full port mode[3]	Nexus data out 0:3	Nexus data out 4:11	f_{SYS} / 4[2, 4]

1 Set NPC_PCR[FPM] = 0.

2 Achieving the absolute minimum MCKO cycle time may require setting the MCKO divider to more than its minimum setting (NPC_PCR[MCKO_DIV]) depending on the actual system frequency being used.

3 Set NPC_PCR[FPM] = 1.

4 This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum MCKO period specification.

4.7.2 Debug: new features

New functionality has been added to the Nexus and JTAG to improve the flexibility of debug.

- The e200z4 core has increased the number of Instruction Address Compare (IAC) registers to eight, compared to the four implemented on the MPC556x e200z6. This allows more instruction breakpoints to be implemented. The e200z4 core also implements new Data Value Compare (DVC) registers to allow debug triggers based upon data address and value matching.
- A mechanism for uncensoring the MCU has been implemented via the JTAG port. The mechanism provides similar functionality to the CAN or eSCI port on the MPC556x, with respect to censorship. Figure 14 shows a high level overview of how a censorship password being supplied serially via TDI, during reset, can un-censor the MCU.

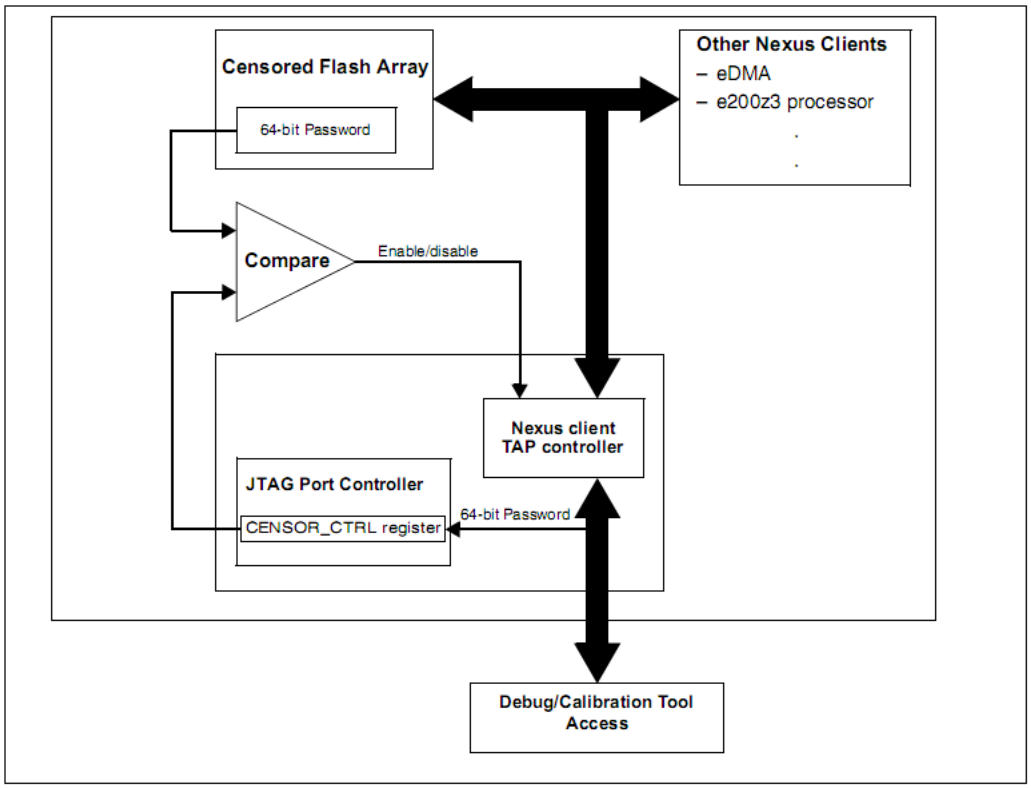


Figure 14. Uncensoring the MCU using JTAG

4.8 Power management controller (PMC)

4.8.1 PMC: software compatibility

The PMC is a new module implemented on the MPC5644A. The default state of the PMC, out of reset, is backwardly compatible with MPC556x software.

4.8.2 PMC: new features

The PMC can be used to integrate previously off-chip functions on-chip. It includes the following features:

- Control of the internal 1.2 V and 3.3 V regulators.
- Programmable Low Voltage Inhibit (LVI) thresholds, which can be configured to trigger an interrupt or a reset event. The programmable LVIs are available on the following power domains:
  - Reset supply pin (VDDEH6)
  - I/O power segment (VDDEH1)
  - 5 V PMC supply (VDDREG)
  - 3.3 V internal regulator / external supply (VDD33)
  - 1.2 V internal regulator / external supply (VDD)
- Trimming of the internal regulator outputs.
  - The output of the internal 1.2 V regulator can be trimmed by ± 150 mV in increments of 20 mV
  - The output of the internal 3.3 V regulator can be trimmed by ± 225 mV in increments of 30 mV

Appendix A Ball map diagrams

Refer to Section 3.1, “Ball map: hardware compatibility” for details on ball map compatibility.

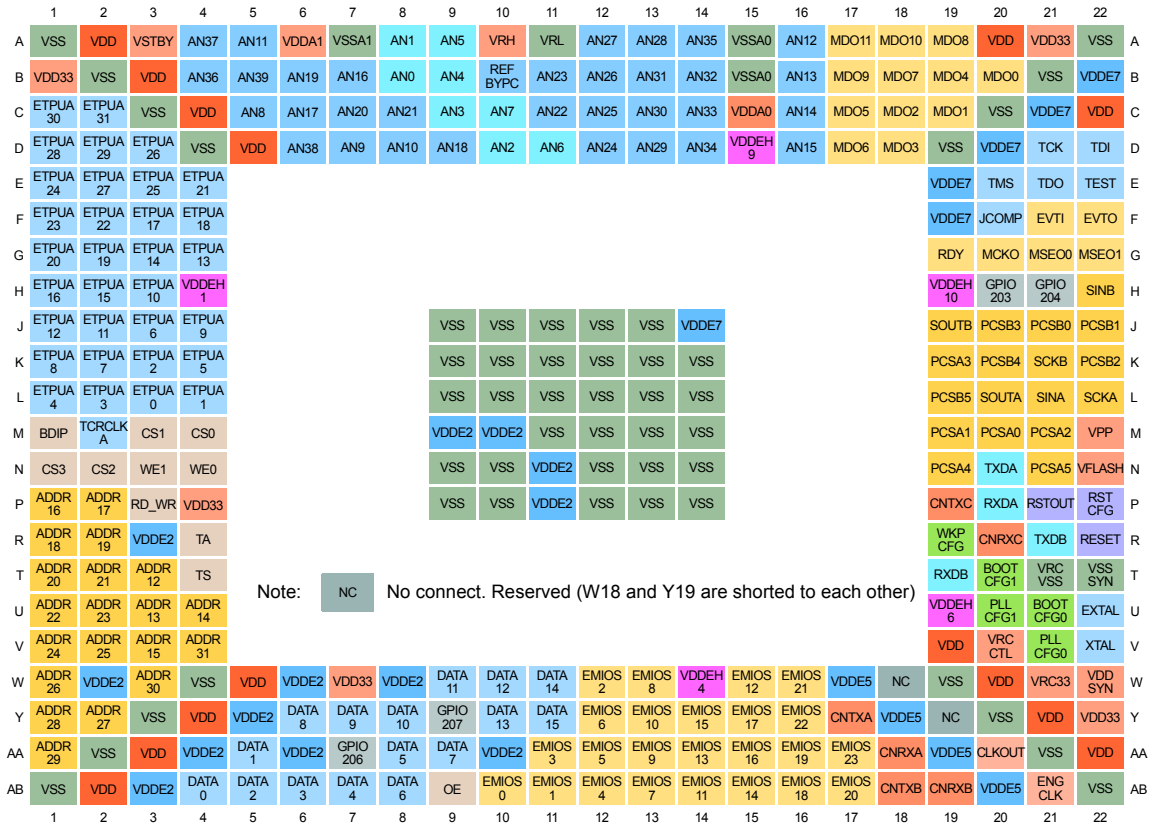
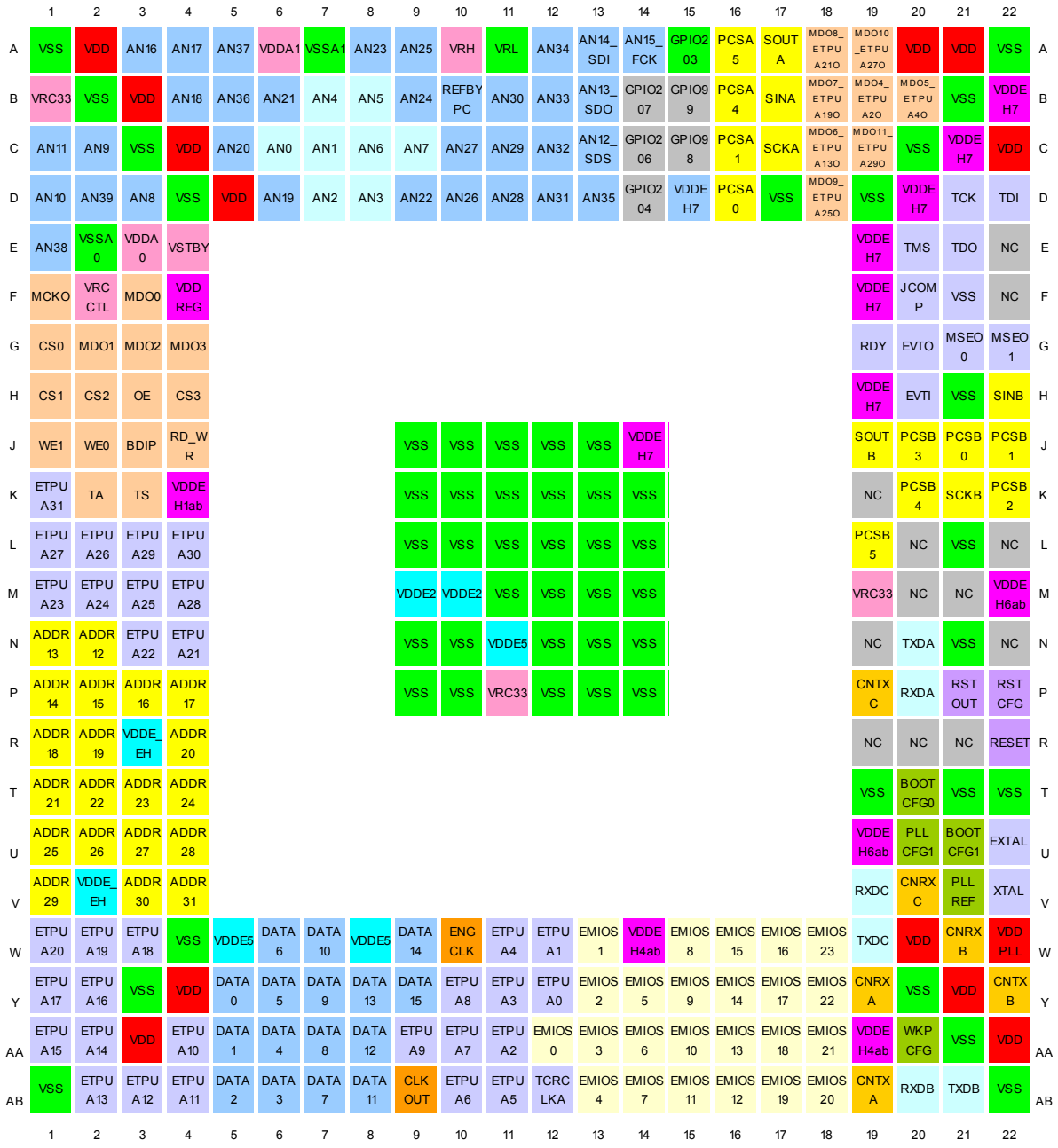


Figure A-1. MPC5565 324 PBGA ball map diagram

NOTE

The MPC5566 is not available in a 324 PBGA footprint.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	VSS	VDD	AN16	AN17	AN37	VDDA1	VSSA1	AN23	AN25	VRH	VRL	AN34	AN14_SDI	AN15_FCK	GPIO203	PCSA5	SOUTA	MDO8_ETPUA21O	MDO10_ETPUA27O	VDD	VDD	VSS	A
B	VRC33	VSS	VDD	AN18	AN36	AN21	AN4	AN5	AN24	REFBYPC	AN30	AN33	AN13_SDO	GPIO207	GPIO99	PCSA4	SINA	MDO7_ETPUA19O	MDO4_ETPUA2O	MDO5_ETPUA4O	VSS	VDDEH7	B
C	AN11	AN9	VSS	VDD	AN20	AN0	AN1	AN6	AN7	AN27	AN29	AN32	AN12_SDS	GPIO206	GPIO98	PCSA1	SCKA	MDO6_ETPUA13O	MDO11_ETPUA29O	VSS	VDDEH7	VDD	C
D	AN10	AN39	AN8	VSS	VDD	AN19	AN2	AN3	AN22	AN26	AN28	AN31	AN35	GPIO204	VDDEH7	PCSA0	VSS	MDO9_ETPUA25O	VSS	VDDEH7	TCK	TDI	D
E	AN38	VSSA0	VDDA0	VSTBY															VDDEH7	TMS	TDO	NC	E
F	MCKO	VRCCTL	MDO0	VDDREG															VDDEH7	JCOMP	VSS	NC	F
G	CS0	MDO1	MDO2	MDO3															RDY	EVTO	MSEO0	MSEO1	G
H	CS1	CS2	OE	CS3															VDDEH7	EVTI	VSS	SINB	H
J	WE1	WE0	BDIP	RD_WR					VSS	VSS	VSS	VSS	VSS	VDDEH7					SOUTB	PCSB3	PCSB0	PCSB1	J
K	ETPUA31	TA	TS	VDDEH1ab					VSS	VSS	VSS	VSS	VSS	VSS					NC	PCSB4	SCKB	PCSB2	K
L	ETPUA27	ETPUA26	ETPUA29	ETPUA30					VSS	VSS	VSS	VSS	VSS	VSS					PCSB5	NC	VSS	NC	L
M	ETPUA23	ETPUA24	ETPUA25	ETPUA28					VDDE2	VDDE2	VSS	VSS	VSS	VSS					VRC33	NC	NC	VDDEH6ab	M
N	ADDR13	ADDR12	ETPUA22	ETPUA21					VSS	VSS	VDDE5	VSS	VSS	VSS					NC	TXDA	VSS	NC	N
P	ADDR14	ADDR15	ADDR16	ADDR17					VSS	VSS	VRC33	VSS	VSS	VSS					CNTXC	RXDA	RSTOUT	RSTCFG	P
R	ADDR18	ADDR19	VDDE_EH	ADDR20															NC	NC	NC	RESET	R
T	ADDR21	ADDR22	ADDR23	ADDR24															VSS	BOOTCFG0	VSS	VSS	T
U	ADDR25	ADDR26	ADDR27	ADDR28															VDDEH6ab	PLLCFG1	BOOTCFG1	EXTAL	U
V	ADDR29	VDDE_EH	ADDR30	ADDR31															RXDC	CNRXC	PLLREF	XTAL	V
W	ETPUA20	ETPUA19	ETPUA18	VSS	VDDE5	DATA6	DATA10	VDDE5	DATA14	ENGCLK	ETPUA4	ETPUA1	EMIOS1	VDDEH4ab	EMIOS8	EMIOS15	EMIOS16	EMIOS23	TXDC	VDD	CNRXB	VDDPLL	W
Y	ETPUA17	ETPUA16	VSS	VDD	DATA0	DATA5	DATA9	DATA13	DATA15	ETPUA8	ETPUA3	ETPUA0	EMIOS2	EMIOS5	EMIOS9	EMIOS14	EMIOS17	EMIOS22	CNRXA	VSS	VDD	CNTXB	Y
AA	ETPUA15	ETPUA14	VDD	ETPUA10	DATA1	DATA4	DATA8	DATA12	ETPUA9	ETPUA7	ETPUA2	EMIOS0	EMIOS3	EMIOS6	EMIOS10	EMIOS13	EMIOS18	EMIOS21	VDDEH4ab	WKPCFG	VSS	VDD	AA
AB	VSS	ETPUA13	ETPUA12	ETPUA11	DATA2	DATA3	DATA7	DATA11	CLKOUT	ETPUA6	ETPUA5	TCRCLKA	EMIOS4	EMIOS7	EMIOS11	EMIOS12	EMIOS19	EMIOS20	CNTXA	RXDB	TXDB	VSS	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure A-2. MPC5644A 324-pin TEPBGA package ballmap

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