Freescale Semiconductor
Application Note

Document Number:AN2613
Rev 0, August 21, 2013

Qorivva MPC5500 Minimum Board Requirements

by: Randy Dees
Application Engineering
Austin, Texas/USA

Contents

1 Introduction

This application note shows recommended example circuits for the Qorivva MPC55xx family of 32-bit microcontrollers (MCU) based on the e200z*x* Power Architecture® cores. Many of these circuits are included on the standard evaluation board for the different devices. In most cases in this application note, the MPC5554 is used in the examples, however, unless otherwise specified, the majority apply to all devices in the family. In addition, some of the MCUs in this family support features that are not available on the MPC5554. Circuits for these options are also shown in this document.

The Qorivva MPC5500 family contains multiple MCUs that were originally designed for automotive powertrain applications and span from the low end MPC5534, with 1 MB of on-chip flash, up to the high end MPC5566 with 3MB of on-chip flash memory. In between are devices with support for a varying number of peripheral devices, including two devices that support FlexRAY. The following table highlights the features available on the different members of the MPC55xx MCU family.

Table 1. Qorivva MPC5500 Family comparison

		MPC5534	MPC5553	MPC5554	MPC5561	MPC5565	MPC5566	MPC5567
Power Architecture Core		e200z3[1]	e200z6	e200z6	e200z6 with VLE	e200z6 with VLE	e200z6 with VLE	e200z6 with VLE
Packages		208 MAPBGA, 324 PBGA	208 MAPBGA, 324 PBGA, 416 PBGA	416 PBGA	324 PBGA	324 PBGA	416 PBGA	324 PBGA, 416 PBGA
Unified Cache		—	8 KB	32 KB[3]	32 KB[4]	8 KB[2]	32 KB	8 KB[2]
Memory Management Unit (MMU)		16 entries	32 entries	32 entries	32 entries	32 entries	32 entries	32 entries
Crossbar		4 x 5	4 x 5	3 x 5	4 x 6	3 x 5[5]	4 x 5	5 x 5
Core Nexus Support		Class 3+	Class 3+	Class 3+	Class 3+	Class 3+	Class 3+	Class 3+
SRAM		64 Kbyte	64 Kbyte	64 Kbyte	192 Kbyte	80 Kbyte	128 Kbyte	80 Kbyte
Flash Memory	Main Array	1 Mbyte[6]	1.5 Mbyte	2 Mbyte[7]	1 Mbyte[7]	2 Mbyte[7]	128 Mbyte[7]	2 Mbyte[7]
	Shadow block	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte
External bus interface (EBI	Data	16-bit	32-bit[8]	32-bit	32-bit	16-bit	32-bit	32-bit[8]
	Address	24-bit	24-bit	24-bit	26-bit	26-bit[9]	26-bit[9]	26-bit[9]
Calibration bus interface		Yes	Partial support	No	Yes	Yes	Yes	Yes
Enhanced direct memory access (eDMA)		32 channels	32 channels	64 channels	32 channels	32 channels	64 channels	32 channels
eDMA Nexus		—	Class 3	Class 3	Class 3	Class 3	Class 3	Class 3
Enhanced serial computer interface (eSCI)	Instances	2	2	2	4	2	2	2
	eSCI A	Y	Y	Y	Y	Y	Y	Y
	eSCI B	Y	Y	Y	Y	Y	Y	Y
	eSCI C	—	—	—	Y	—	—	—
	eSCI D	—	—	—	Y	—	—	—
Controller Area network (FlexCAN)	Instances	2	2	3	2	3[10]	4[10]	5[10]
	CAN A	64 buffers	64 buffers	64 buffers	64 buffers	64 buffers	64 buffers	64 buffers
	CAN B	—	—	64 buffers	—	64 buffers	64 buffers	64 buffers
	CAN C	64 buffers	64 buffers	64 buffers	64 buffers	64 buffers	64 buffers	64 buffers
	CAN D	—	—	—	—	—	64 buffers	64 buffers
	CAN E	—	—	—	—	—	—	64 buffers
Deserial to serial peripheral interface (DSPI)	Instances	3	3	4	2	3	4	3
	DSPI A	—	—	Y	—	—	Y	—
	DSPI A	Y	Y	Y	Y	Y	Y	Y
	DSPI C	Y	Y	Y	Y	Y	Y	Y
	DSPI D	Y	Y	Y	—	Y	Y	Y
enhanced Modular Input/ Output System (eMIOS)		24 channel	24 channel	24 channel	24 channel	24 channel	24 channel	24 channel
Enhanced Time	Channels	32 channel	32 channel	64 channel	0 channel	32 channel	64 channel	32 channel
	eTPU A	Y	Y	Y	Y	Y	Y	Y

Table continues on the next page...

Table 1. Qorivva MPC5500 Family comparison (continued)

		MPC5534	MPC5553	MPC5554	MPC5561	MPC5565	MPC5566	MPC5567
Processing Unit (eTPU)	eTPU B	—	—	Y	—	—	Y	—
	Code Memory	12 Kbyte	12 Kbyte	16 Kbyte	0 Kbyte	12 Kbyte	20 Kbyte	12 Kbyte
	Parameter SRAM	2.5 Kbyte	2.5 Kbyte	3 Kbyte	0 Kbyte	2.5 Kbyte	4 Kbyte	2.5 Kbyte
	Nexus	Class 3	Class 3	Class 3	—	Class 3	Class 3	Class 3
Interrupt Controller (INTC)		210 channel	210 channel	308 channel	231 channel	231 channel	320 channel[11]	231 channel
enhanced Queued Analog-to-Aigital Converter (eQADC)	Channels	40 channel	40 channel	40 channel	40 channel	40 channel	40 channel	40 channel
	ADC0	Y	Y	Y	Y	Y	Y	Y
	ADC1	Y	Y	Y	Y	Y	Y	Y
Fast Ethernet controller (FEC)		—	Y[12]	—	—	—	Y	Y[13]
FlexRay		—	—	—	Y	—	Y	—
FlexRay Nexus		—	—	—	Class 3	—	Class 3	—
Phase lock loop (FMPLL)		FM	FM	FM	FM	FM	FM	FM
Maximum system frequency		82 MHz[14]	132 MHz	132 MHz	135 MHz[15]	135 MHz	147 MHz[16]	135 MHz
Crystal range		8-20 MHz	8-20 MHz	8-20 MHz	8-20, 40 MHz	8-20 MHz	8-20 MHz	8-20, 40 MHz
Voltage regulator		Y	Y	Y	Y	Y	Y	Y

1. All e200z3 cores support the Variable Length Encoded (VLE) Instruction set.
2. 2-way associative
3. 8-way associative
4. 4-way or 8-way associative
5. The actual crossbar is implemented as a 5 x 5 crossbar with two unused ports.
6. 16-byte flash page size for programming.
7. 32-byte flash page size for programming.
8. May not be externally available in all packages.
9. Either ADDR[8:31] or ADDR[6:29] can be selected.
10. Updated FlexCAN module with optional individual receive filters.
11. Although this device has a maximum of 329 interrupts, the logic requires that the total number of interrupts be divisible by four. Therefore, the total number of interrupts specified for this device is 332.
12. The FEC signals are multiplexed with data bus pins DATA[16:31].
13. The FEC signals are shared with the calibration bus.
14. 80 MHz + 2% FM
15. 132 MHz + 2% FM
16. 144 MHz + 2% FM

The figure below shows a block diagram of a typical evaluation board and how some of the peripherals are connected to the MCU. This also shows using the Freescale MC33730 power supply device.

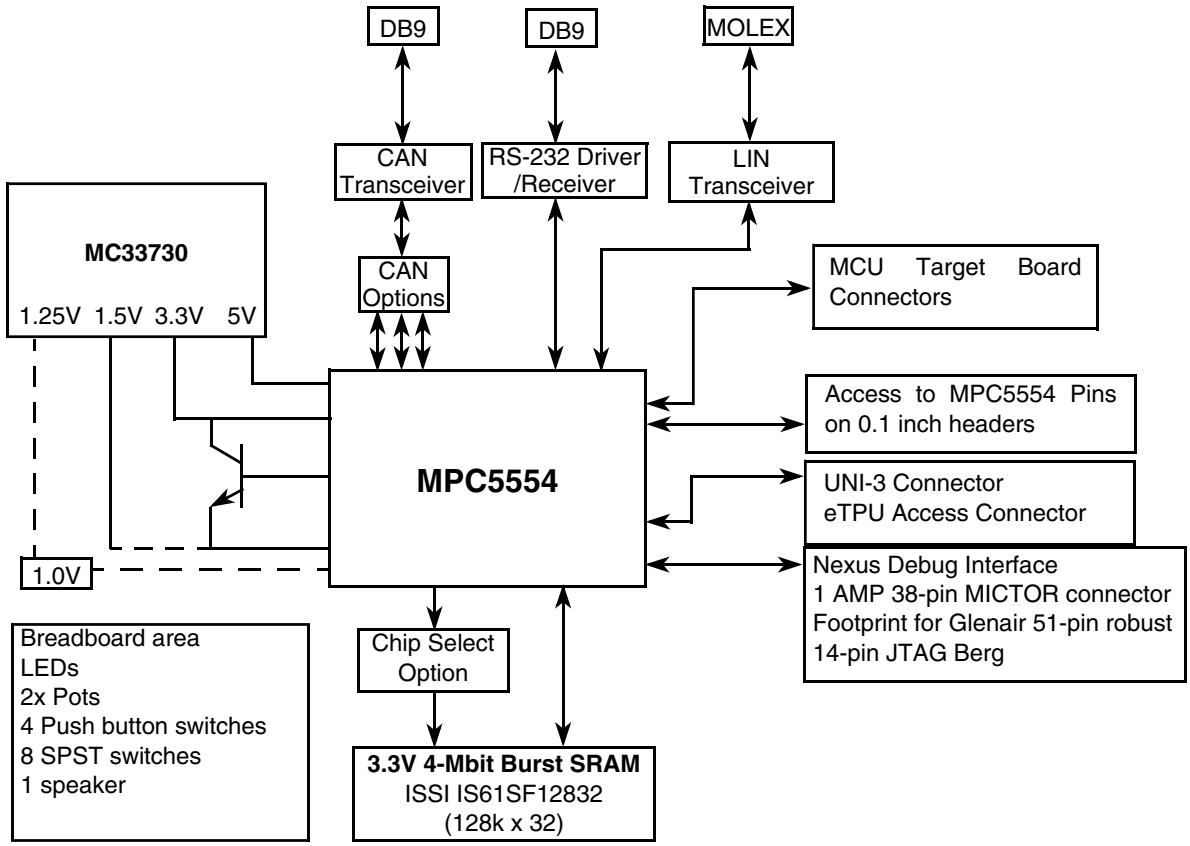


Figure 1. Typical evaluation board block diagram

1.1 MPC5500 Packages

The MPC5500 devices are available in multiple packages to address the size and Input/output requirements of different types of systems. All of these packages are Plastic Ball Grid Array (PBGA) or Mold Array Process Ball Grid Array (MAP-BGA), Not all devices are available in all packages. The following table shows the package options for the different devices.

Table 2. MPC5500 device package options

Device	208 MAPBGA	324 PBGA	416 PBGA
	17 mm x 17 mm	23 mm x 23 mm	27 mm x 27 mm
MPC5534	√	√	—
MPC5553	√	√	√
MPC5554	—	—	√
MPC5561	—	√	—
MPC5565	—	√	—
MPC5566	—	—	√
MPC5567	—	√	√

2 Reset Configuration

Some operating features of the device are configured during reset. Depending on the value of the Reset Configuration pin ($\overline{\text{RSTCFG}}$), either a default configuration is selected or external pins provide the configuration information. $\overline{\text{RSTCFG}}$ has an internal pull up that will select the default settings unless driven from an external circuit or pulled down with an external device strong enough to overcome the internal pull up. The following features are controllable via the reset configuration pins:

- Default configuration or externally controlled configuration ($\overline{\text{RSTCFG}}$)
- Boot mode: internal flash, external memory, or serial boot (BOOTCFG[0:1])
- Clock Configuration: crystal oscillator or external reference clock (PLLCFG[0:1]), plus clock range (PLLCFG[2][1])
- Timer channel default pull (up or down) direction (WKPCFG)

The configuration pins (PLLCFG[0:1/2] and BOOTCFG[0:1]) are internally latched four clocks prior to the MCU negating $\overline{\text{RSTOUT}}$ if $\overline{\text{RSTCFG}}$ is asserted. WKPCFG is always latched four clocks prior to $\overline{\text{RSTOUT}}$ negation and is not controlled by the $\overline{\text{RSTCFG}}$ pin.

Depending on the system requirements, there are four recommended circuit options to support the reset configuration of the device. These are shown in the following table and are each described in later sections of this document.

Table 3. Recommended configuration circuit options

Desired Reset Configuration Option	$\overline{\text{RSTCFG}}$ value	Clock Source	Boot location	Notes
Absolute minimum reset configuration (see Minimum (default) RESET configuration circuit (most commonly used))	1 (high)	Internal crystal oscillator	Internal flash	Uses internal crystal oscillator, boot from internal flash
Full reset configuration control[1] (see External $\overline{\text{RESET}}$ configuration with optional GPIO on config pins)	0 (low)	Internal crystal oscillator or external reference clock	Internal flash or external memory (selectable based on desired configuration)	This configuration is required if the configuration pins[2] are used for General Purpose Input/Outputs (GPIO)
Recommended minimum configuration when using an external reference clock with GPIO on config pins (see Minimum required circuitry for external reference clock mode (with optional GPIO))	0 (low)	External reference clock	Internal flash or external memory (selectable based on desired configuration)	Optionally, GPIO can be used with additional circuitry
Absolute minimum configuration for an external reference clock without GPIO on config pins (see Absolute minimum RESET configuration circuit for external clock (GPIO on config pins not allowed))	0 (low)	External reference clock	Internal flash or external memory (selectable based on desired configuration)	The Pad Configuration Registers (PCR) for the configuration pins must be left in their default states (GPIO not allowed on the configuration pins).

1. Not available on all devices.

1. Recommended for evaluation boards or initial prototypes to allow different configurations to be set.
2. RSTCOFG, PLLCFG[0:1], and/or BOOTCFG[0:1]

The following table shows the default configuration that is selected if RSTCFG is negated (high).

Table 4. Default (RSTCFG = 1) configuration

Signals	Value	Selection
BOOTCFG[0:1]	0b00	Boot from internal flash
PLLCFG[0:1]	0b10	Use crystal oscillator

RSTCFG controls selection of either the default configuration or an external configuration as shown in the following table.

Table 5. Default (internal) versus external configuration control

RSTCFG Value	Configuration mode
1	Default (internal) boot mode selected with a crystal oscillator reference. This provides the same configuration as setting BOOTCFG[0:1]=0b00 and PLLCFG[0:1]=0b01
0	The values of BOOTCFG[0:1] and PLLCFG[0:1] control the boot and clock mode configuration

The following table shows the possible configurations of the memory boot mode.

Table 6. Boot memory configuration options

BOOTCFG[0]	BOOTCFG[1]	Boot mode
0	0	Boot from the internal flash memory (default when RSTCFG = 1)
0	1	Boot from FlexCAN or eSCI
1	0	Boot from the external memory (single master, with no arbitration)
1	1	Boot from the external memory (multi-master mode with external bus arbitration). This mode is only supported on the MPC5554. It is not supported on other devices.

The following table shows the options for the clock configuration that are controlled out of reset. On devices that support PLLCFG[2], PLLCFG[2] is not latched and controls the predivider value of the PLL. PLLCFG[2] should only be high if a 40 MHz crystal is used.

Table 7. PLL clock configuration

PLLCFG[0]	PLLCFG[1]	PLL Clock mode
0	0	Bypass mode
0	1	Normal mode with external reference clock
1	0	Normal mode with external crystal reference (uses internal oscillator). This is the default mode if RSTCFG = 1.
1	1	1:1 mode[1]

1. This mode is intended for use in dual controller systems only.

The default state of the enhanced Timing Processing Unit (eTPU) and the enhanced Modular Input/Output System (eMIOS) timer pins is controlled by the weak pull configuration pin (WKPCFG) as shown in the following table.

WKPCFG	Weak Pull Configuration
0	eTPU and eMIOS pins have weak pull downs enabled.
1	eTPU and eMIOS pins have weak pull ups enabled.

NOTE

Not all eTPU and eMIOS pins are controlled by the WKPCFG pins. See the pin descriptions in the device Data Sheet and Reference Manual.

During the internal power on reset (POR) of the MPC5500 devices, the reset output pin ($\overline{\text{RSTOUT}}$) floats. A pull resistor on $\overline{\text{RSTOUT}}$ is required to control external circuitry during POR. Normally, a pull down should be used on $\overline{\text{RSTOUT}}$ to hold external circuitry in reset during POR. However, if an external configuration is required (for PLLCFG[1:0] and BOOTCFG[1:0]), then care needs to be taken. A possible, but extremely rare, misconfiguration can occur when the internal POR negates[2]. There are multiple ways to address the requirements for external configuration depending on the system requirements such as external clock use and GPIO on the configuration pins. The examples in the external configuration subsections of this document ensure that the errata will not be seen in the target system. Depending on the external configuration circuitry, if $\overline{\text{RSTOUT}}$ has a pull up resistor to pull $\overline{\text{RSTOUT}}$ up during POR, then a conditioned external reset out ($\overline{\text{ERSTOUT}}$) may be required for external devices that require $\overline{\text{RSTOUT}}$ to be low even during the internal POR time of the MCU. Freescale evaluation boards provide $\overline{\text{ERSTOUT}}$ that ANDs $\overline{\text{RESET}}$ and $\overline{\text{RSTOUT}}$ together. (The $\overline{\text{ERSTOUT}}$ circuit is shown in external reset configuration sections, but can be used with the default [internal] reset configuration.)

The following figure shows the configuration pins under different power up scenarios. During POR, $\overline{\text{RSTOUT}}$ floats. The $\overline{\text{RESET}}$ input to the MCU must be driven low by external Low Voltage Detect circuit before POR negates. The POR voltage trip point is specified in the device data sheet (POR will negate on the MPC5554 between 1.1 and 1.35 volts for the 1.5 V (nominal) supply. Additionally, the device will be kept in the POR state until both the $\overline{\text{RESET}}$ pin power supply (VDDEH6[3]) and VDDSYN are between 2.0 V and 2.85 V. (VDDSYN will also assert the internal POR once it is powered to 0.3 volts.)

NOTE

External low voltage detect (LVD) circuits must be used on all of the external power supplies to ensure proper operation of the device. The external LVD circuitry must ensure that the power supplies are within the recommended operating voltage prior to releasing the $\overline{\text{RESET}}$ input to the MCU.

2. See errata number e488 (ERR000488/e488) on the device errata list.
3. Although VDDEH6 is normally a 5 V supply, it can be used at a nominal voltage of 3.3 volts. Therefore the POR low voltage detect must support 3.3 V operation, as well as 5 V operation.

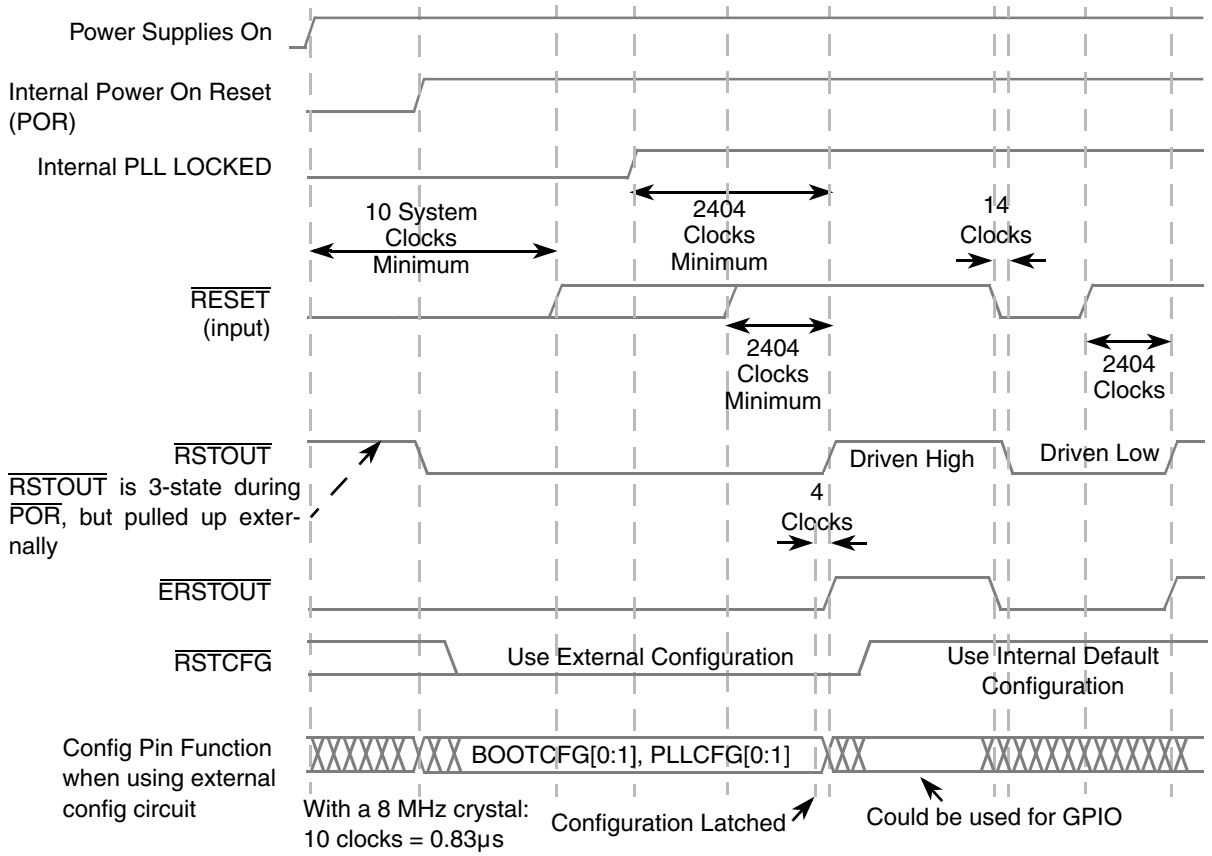


Figure 2. External reset configuration and conditioned $\overline{\text{RSTOUT}}$ timing

In the figure above, both a default configuration ($\overline{\text{RSTCFG}}$ = 1) and an external configuration ($\overline{\text{RSTCFG}}$ = 0) are shown.

$\overline{\text{RESET}}$ must be asserted for at least 10 clocks and includes a two clock glitch filter circuit. $\overline{\text{RSTOUT}}$ will negate 2404 clocks after either $\overline{\text{RESET}}$ is negated or the system Phase Lock Loop (PLL) locks, whichever occurs last. If the device is out of reset ($\overline{\text{RSTOUT}}$ negated) and $\overline{\text{RESET}}$ is asserted, $\overline{\text{RSTOUT}}$ will assert after 14 system clocks (two clock glitch filter + 10 clock minimum $\overline{\text{RESET}}$ assertion time + two clocks for the reset state machine).

NOTE

All reset timing is based on the internal system clock. The internal system clock can either be the "limp" clock (Self-clock mode [SCM] frequency) or the PLL frequency depending on which is active and selected for use by the device.

2.1 Internal Power On Reset

Internal to each of the MPC55xx devices, a Power On Reset circuit is included to ensure that the internal logic of the device and the states of all of the device pins is in a predictable state until a minimum set of the power supplies are near to an operational voltage. Not every power supply input to the device is monitored, only the three most critical supplies are monitored. These supplies are shown in the following table.

Table 9. Critical POR power supplies

Power Supply Pin(s)	Power supply description
VDD	Device internal low voltage circuit supply
VDDSYN	Phase Lock Loop and Crystal power supply
VDDEH6	Power supply for the Reset pin

Below is an extract from a typical[4] data sheet for the specifications for the voltage requirements for each of the critical power supplies. The actual and latest device data sheet should be consulted. Until all of these supplies are greater than the specifications shown, the internal circuitry and the pads are kept in a safe state.

Table 10. POR specifications

Specification	Characteristic		Symbol	Minimum	Maximum	Units
1	1.5 C (V_{DD}) POR[1]	Negated (ramp up)	V_{POR15}	1.1	1.35	V
		Asserted (ramp down)		1.1	1.35	
2	3.3 V (VDDSYN) POR[2]	Asserted (ramp up)	V_{POR33}	0.0	0.30	V
		Negated (ramp up)		2.0	2.85	
		Asserted (ramp down)		2.0	2.85	
		Negated (ramp down)		0.0	0.30	
3	RESET pin Supply (V_{DDEH6}) POR	Negated (ramp up)	V_{POR5}	2.0	2.85	V
		Asserted (ramp down)		2.0	2.85	

1. The internal POR signals are V_{POR15}, V_{POR33}, and V_{POR5}. On power up, assert $\overline{\text{RESET}}$ before the internal POR negates. $\overline{\text{RESET}}$ must remain asserted until the power supplies are within the operating conditions as specified in DC Electrical Specifications table of the Data Sheet. On power down, assert $\overline{\text{RESET}}$ before any power supplies fall outside the operating conditions and until the internal POR asserts.
2. The input low voltage (VIL_S) is guaranteed to scale with V_{DDEH6} down to V_{POR5}

There are no power supply sequencing requirements, however, the state of the Input/output pins does depend on the order of the power supplies and the state of the internal POR[5]. This may dictate a power supply sequence if the pin state shown in the tables below (a typical extract is shown) is not desired. These states are shown in the device data sheet. The high voltage (medium and slow speed) pins have different supply requirements than the higher speed, low voltage pins. This first table is for the high speed pins (low voltage pins [generally 3.3 V typical or less]).

Table 11. Pin status for Fast Pads During the Power Sequence

V_{DDE}	V_{DD33}	V_{DD}	POR	Pin state for the fast pads
Low	—	—	Asserted	Low
V_{DDE}	Low	Low	Asserted	High
V_{DDE}	Low	V_{DD}	Asserted	High
V_{DDE}	V_{DD33}	Low	Asserted	High impedance (Hi-Z)
V_{DDE}	V_{DD33}	V_{DD}	Asserted	Hi-Z
V_{DDE}	V_{DD33}	V_{DD}	Negated	Functional

This table shows the medium and slow pins.

4. This extract is from the MPC5554 Data sheet, revision 4, dated May 2012.
5. The POR state is determined by the table able.

Table 12. Pin status for Medium and Slow Pads During the Power Sequence

V_{DDEH}	V_{DD}	POR	Pin status for Medium and Slow Pad Output Driver mad_mh (medium) pad_sh (slow)
Low	—	Asserted	Low
V_{DDEH}		Asserted	Hi-Z
V_{DDEH}	V_{DD}	Asserted	Hi-Z
V_{DDEH}	V_{DD}	Negated	Functional

2.2 Minimum (default) RESET configuration circuit (most commonly used)

The figure below shows the minimum circuitry required if the internal default reset configuration is used ($\overline{\text{RSTCFG}}$ = 1). This is the most commonly used configuration.The default reset configuration uses an internal crystal oscillator (with an external crystal reference) and searches the internal flash for a valid reset configuration half word (RCHW) BOOTID (RCHW[BOOTID] = 0x5A). If no valid RCHW is found, the device attempts a serial boot (either CAN or SCI). A pull down should be included on $\overline{\text{RSTOUT}}$ since this pin floats during the internal power on reset (POR). This allows $\overline{\text{RSTOUT}}$ to be low during POR for external devices. A pull up resistor must be included on $\overline{\text{RESET}}$ since it could be driven from multiple open drain/open collector devices. The internal pull up on $\overline{\text{RESET}}$ may not be sufficient to pull up all external devices or even to ensure that that $\overline{\text{RESET}}$ will negate in time for proper configuration of the device. The circuit in this figure is for devices without a PLL Config 2 (PLLCFG[2]) pin using an 8 to 20 MHz crystal. This circuit can also be used on devices with a PLLCFG[2] pin, if PLLCFG[2] is tied low (to use an 8 to 20 MHz crystal).

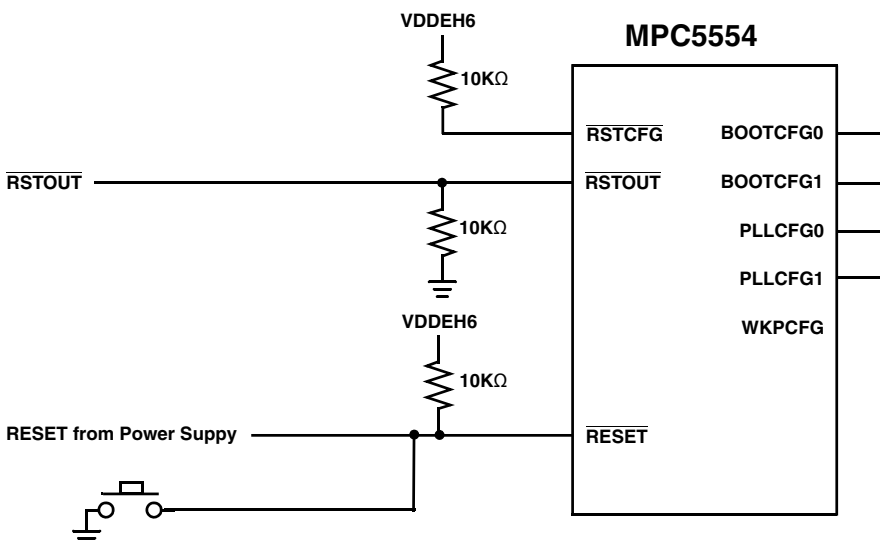


Figure 3. Absolute minimum reset configuration circuit for the MPC5500 devices (without FlexRAY)

On devices with a PLLCFG[2] pin (MPC5567 and MPC5561), the following minimum circuit can be used with a 40 MHz crystal.

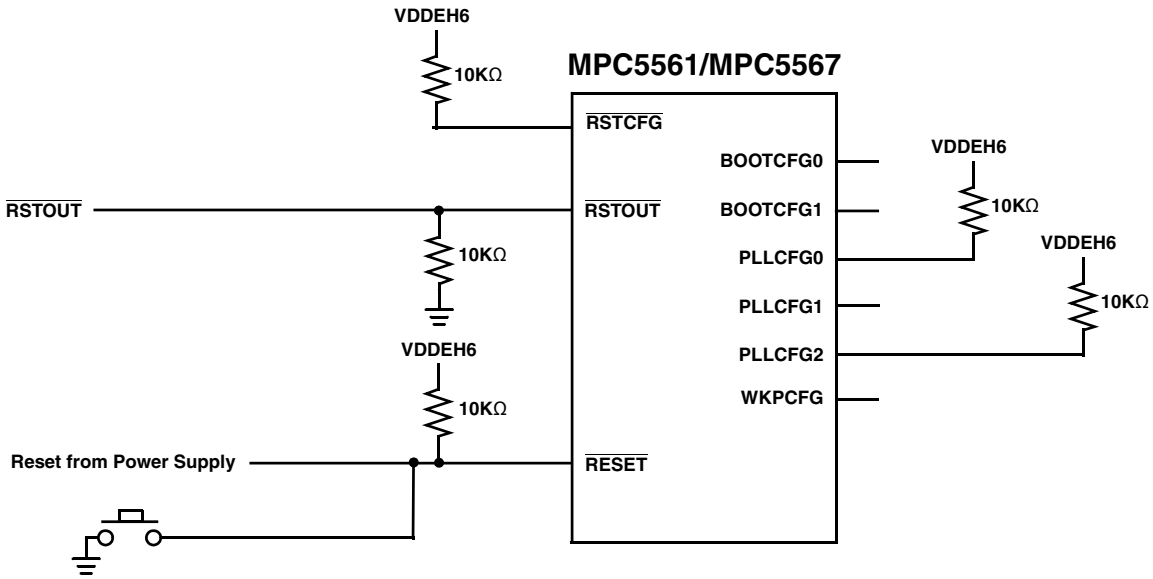


Figure 4. Absolute minimum reset configuration for a 40 MHz crystal

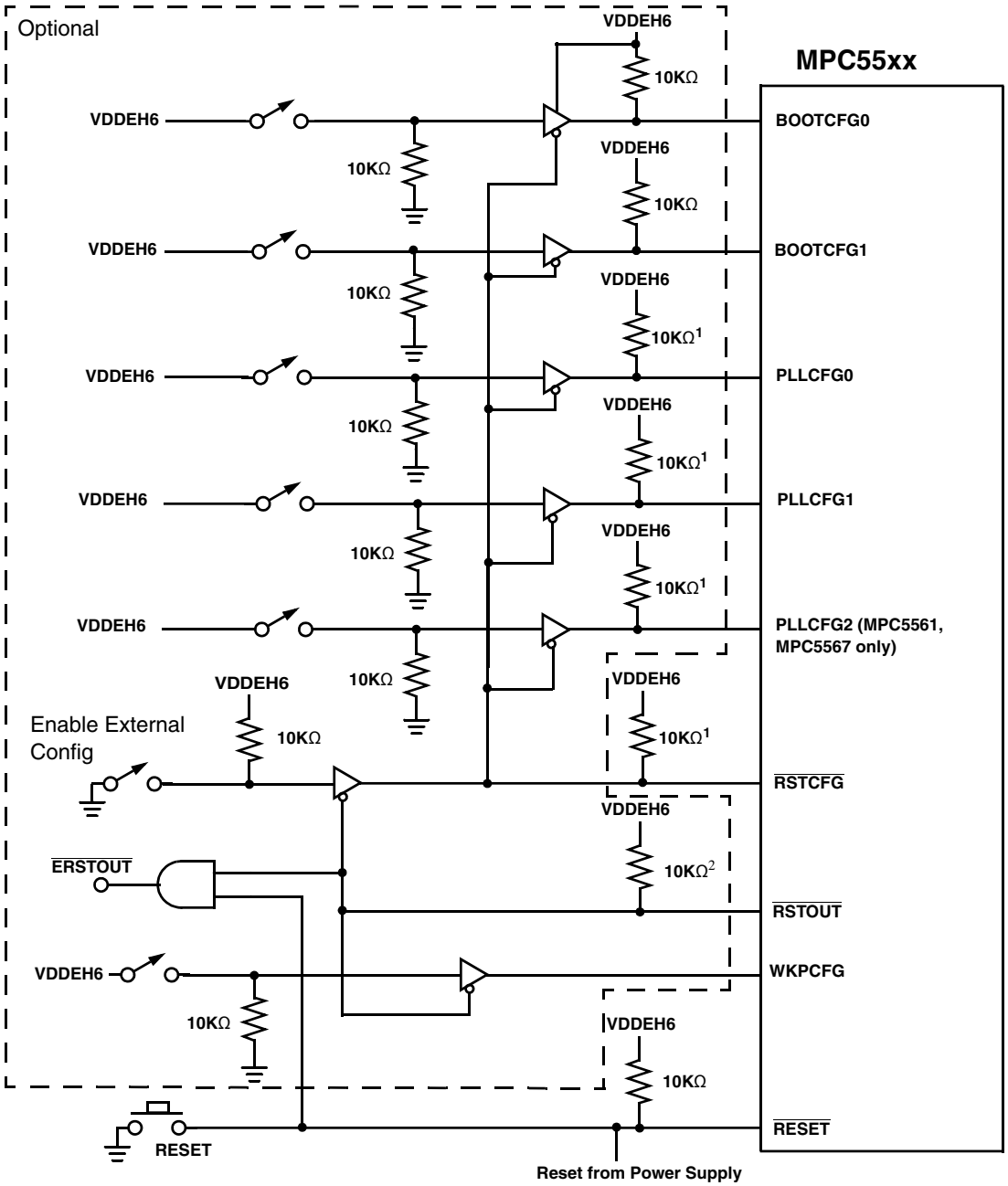
NOTE

The PLLCFG[2] pin can not be used as a general purpose I/O pin. It is always the PLLCFG[2] function, the feature is not latched by reset.

2.3 External $\overline{\text{RESET}}$ configuration with optional GPIO on config pins

The figure below shows the circuitry required to use an external configuration, especially when using the external configuration and using the configuration pins as General Purpose Input/Output (GPIO) after reset. An external configuration is required when using an external clock reference source or when booting from external memory (feature not available on all devices). This circuit has a pull up on $\overline{\text{RSTOUT}}$ in order to disable driving the reset configuration during the internal POR and during normal operation. An AND gate is included in this circuit (with $\overline{\text{RESET}}$ [in] and $\overline{\text{RSTOUT}}$ on its inputs) to generate a reset for any other circuitry in the system that requires a reset signal. On the evaluation boards, this reset ($\overline{\text{ERSTOUT}}$) only drives the reset LED and the DP83848 Ethernet Physical interface device (if applicable), but can be used if additional peripherals are added to the board that require a reset. This circuit (below) is required to sequence $\overline{\text{RSTCFG}}$ and the PLLCFG[0:1] pins. This addresses the possible issue from errata e488. $\overline{\text{RSTCFG}}$ is held high until the internal POR[6] negates and then applies the reset configuration to the configuration pins.

6. All of the MPC5500 Family devices contain a rough Power On Reset circuit to hold internal circuits in reset until sufficient voltage is available on all of the power supplies.See Internal Power On Reset.



Notes:
1. This pull up is required, even if the internal reset configuration word is used.
2. The10K resistor on RSTOUT should be a pull down if the optional external configuration circuitry is not used.

Figure 5. External Configuration circuitry

2.3.1 Using configuration pins as GPIO

If the external configuration pins to be used for General Purpose Input or Outputs (GPIO) and the external configuration pins are used for configuring the device modes ($\overline{\text{RSTCFG}}$ = 0), additional circuitry is required to that the configuration pins are in the proper state for configuring the device. The GPIO functionality should be gated by the conditioned external $\overline{\text{ERSTOUT}}$.

NOTE

Care must be taken to ensure that the configuration pins (RSTCFG, PLLCFG[0:2], and BOOTCFG[0:1]) are in the proper state while $\overline{\text{RESET}}$ is asserted.

In the following circuit, $\overline{\text{RSTOUT}}$ is used to gate the $\overline{\text{RSTCFG}}$ pin. This circuit depends on the fact that $\overline{\text{RSTOUT}}$ negates internally before $\overline{\text{RSTCFG}}$ is asserted when using an external configuration.

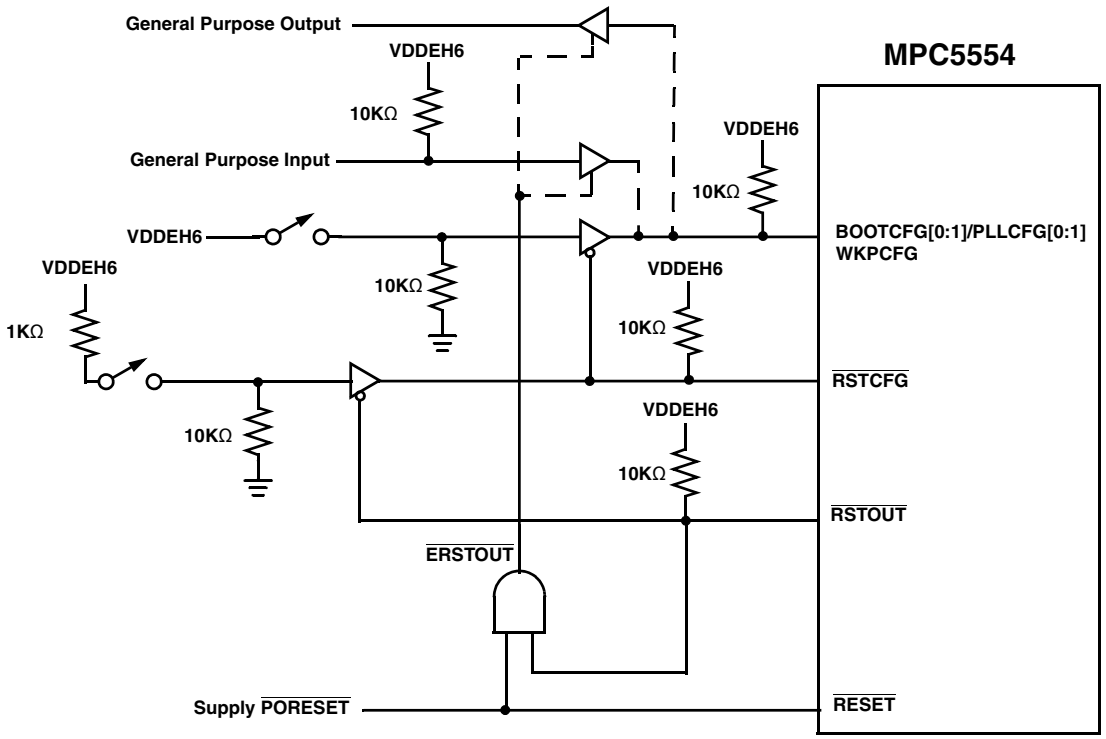


Figure 6. Reset configuration with GPIO circuit (not all pins shown for simplicity)

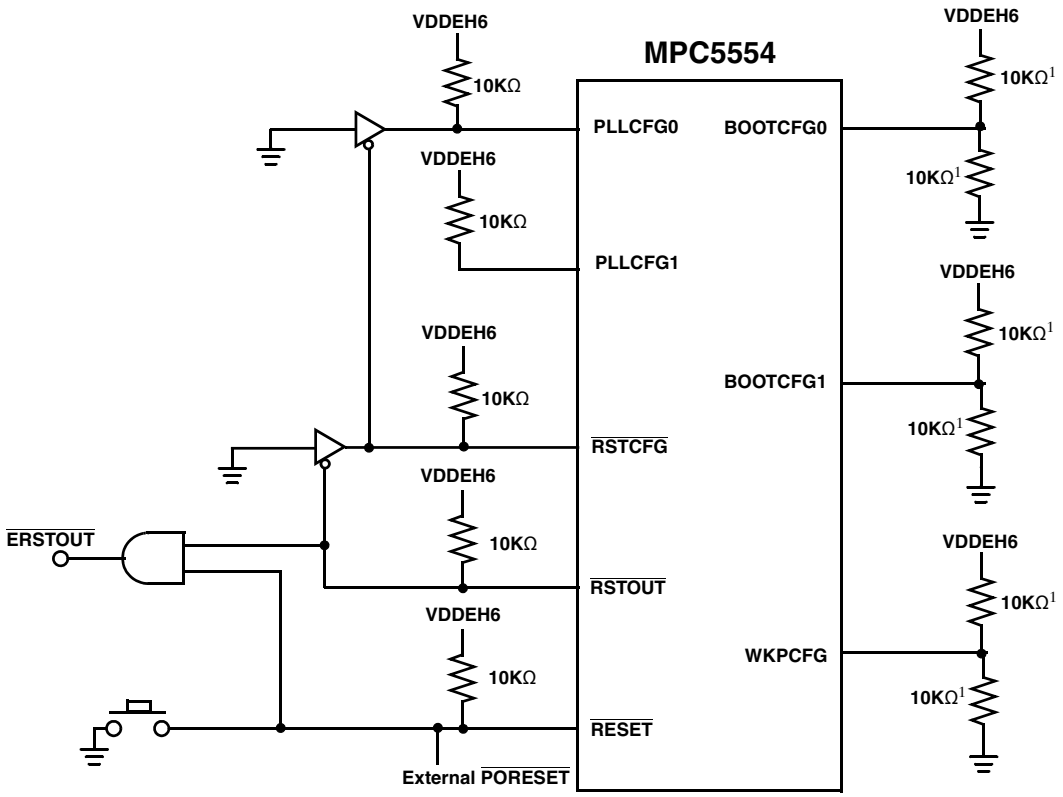
The circuit shown on the WKPCFG is only needed if the WKPCFG pin is to be used for GPIO following reset. If the GPIO function is not required for this pin, it can just be pulled up or down depending on user requirements.

2.4 Minimum required circuitry for external reference clock mode (with optional GPIO)

When using the MPC5500 devices with an external reference clock (PLLCFG[0:1]=0b01), extra circuitry is required to ensure that the system clock will be configured properly out of power-on reset (POR - internal MPC5500 POR circuit). During POR, the default value (default POR configuration) of the PLLCFG[0:1] bits are set to 0b10 and $\overline{\text{RSTCFG}}$ is high. External reference clock mode requires that the PLLCFG[0:1] bits have a value of 0b01 and therefore requires the external configuration. External circuitry is required to ensure that the value of 0b00 is not seen on the internal version of the PLLCFG[0:1] pins during the change from the default POR configuration to the external configuration.

The figure below shows the minimum circuitry required to select the external reference clock mode of the PLL and optionally allows use of the configuration pins as General Purpose Input/Outputs (GPIO). The BOOTCFG[0:1] pins can be pulled up or down depending on the boot memory configuration required by the user. This circuitry initially selects the default POR configuration. After the internal POR negates, $\overline{\text{RSTOUT}}$ will begin to drive and will enable the change to the external configuration, which then switches PLLCFG[0] from a high to a low.

In the following circuit, $\overline{\text{RSTOUT}}$ is used to gate the $\overline{\text{RSTCFG}}$ pin. This circuit depends on the fact that $\overline{\text{RSTOUT}}$ negates internally before $\overline{\text{RSTCFG}}$ is asserted when using an external configuration.



Notes:
1. Populate these resistors as required to select the boot mode (BOOTCFG[0:1]) and the WKPCFG value.

Figure 7. Minimum reset configuration pin circuitry for external clock mode

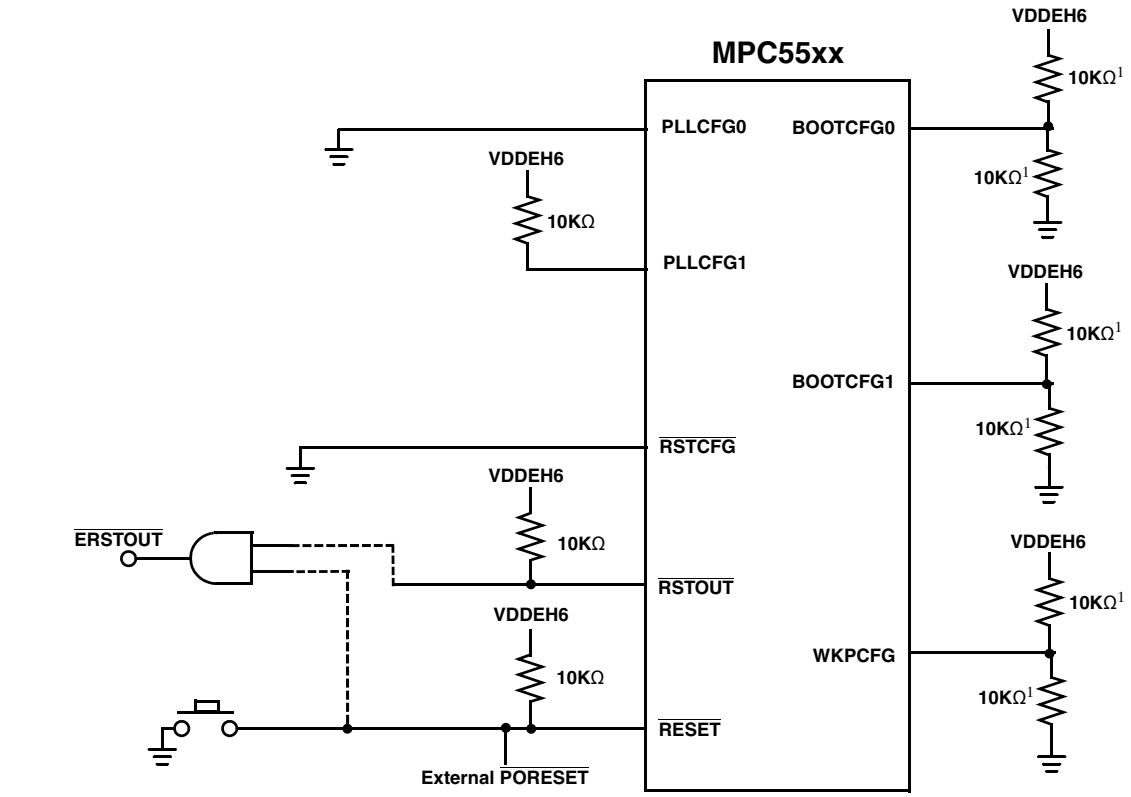
See the previous section for circuitry to isolate the GPIO functions from the configuration functions.

2.5 Absolute minimum RESET configuration circuit for external clock (GPIO on config pins not allowed)

The figure below shows the absolute minimum circuitry required when using an external clock reference. The device configuration pins cannot be used as General Purpose Input/Output (GPIO) when using this absolute minimum circuitry. Software must not change the default settings of the Pad Configuration Registers (PCR) for the Phase Lock Loop (PLL) configuration pins (PLLCFG[2:0]). In this case, the reset configuration pin ($\overline{\text{RSTCFG}}$) can be pulled low all of the time.

NOTE

With this configuration, the GPIO circuitry on the PLLCFG[0:1] configuration pins must not be enabled by software.



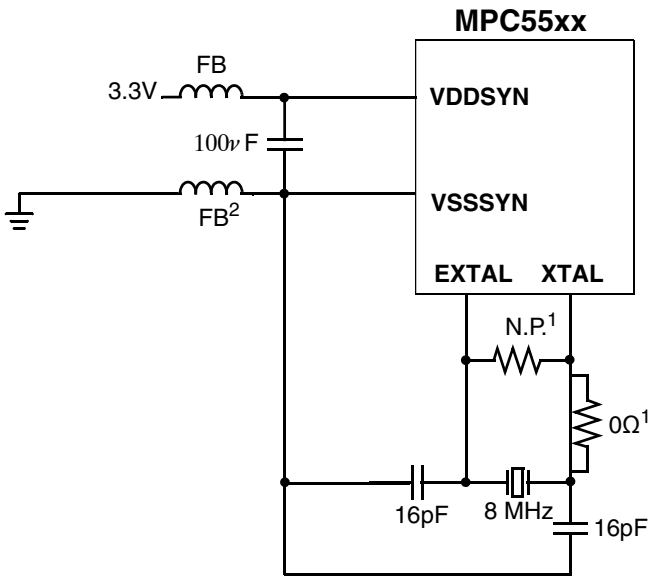
Notes:
1. Populate these resistors as required to select the boot mode (BOOTCFG[0:1]) and the WKPCFG value.

Figure 8. Absolute minimum reset configuration circuit for the MPC5500 devices (No GPIO on config pins)

$\overline{\text{ERSTOUT}}$ is an optional signal depending on system requirements. Some systems may use this signal to disable external devices while the MCU is in reset such as external memories or even external driver circuits.

3 Clock Circuitry

The external crystal for the Frequency Modulated Phase Lock Loop (FMPLL) must be in the range of 8 to 20 MHz for most of the MPC5500 devices and connected to the EXTAL and XTAL pins. The Freescale evaluation boards for these devices typically have an 8 MHz crystal oscillator, which is multiplied by the FMPLL internal circuitry to obtain the desired operating speed. Some boards (devices that support FlexRay) use a 40 MHz crystal. Typical connections are shown in the following figure.



1. Provisions for an external feedback resistor and a series resistors should be made on board layouts. The feedback resistor is not currently required and should not be populated. The series resistor should be a 0 Ω resistor. On the Freescale evaluation boards, the series resistor is implemented as a cut-away options with pads for a resistor.
2.The VSSSYN Ferrite Bead (FB) is not required if VSSSYN is connected directly to a ground plane (not just a ground signal trace).

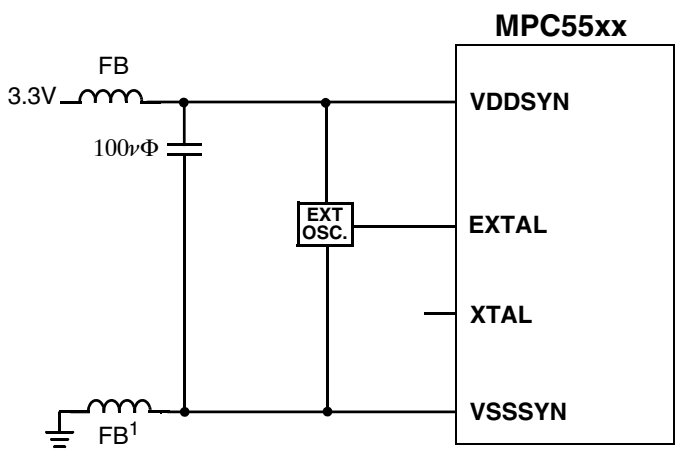
Figure 9. MPC5500 VDDSYN and crystal connections (8-20 MHz crystals)

NOTE

The oscillator circuit should be placed as close as possible to the MCU. In order to minimize signal degradation, the circuitry should all be placed on the same PCB layer avoiding unnecessary vias where possible. The VSSSYN trace should be used as a shield around the crystal components.

VSSSYN should be used as a shield for the oscillator and then connected to the ground plane at the crystal load capacitors.

The figure below shows the connections when using an external reference clock. When using an external reference clock, XTAL should be left open.



1. The VSSSYN Ferrite Bead (FB) is not required if VSSSYN is connected to a ground plane (not just a ground signal trace).

Figure 10. External Clock reference example

Some devices, such as the MPC5567 and the MPC5561 that support FlexRAY, also allow for a 40 MHz external crystal configuration. These devices include an additional configuration pin (PLLCFG[2]) to select between the 8-20 MHz crystal or the 40 MHz crystal. PLLCFG2 does not exist and was used as VRCVSS on other devices (that do not support the 40 MHz option). To select the 40 MHz option, PLLCFG[2] should be pulled or driven high.

NOTE

Setting PLLCFG[2] high forces the Predivider (set to divide-by-two) in the PLL to be selected by default, making the input to the PLL the same as the 8-20 MHz option.

When using the 40 MHz crystal, the buffered crystal frequency is available to be selected for the FlexRAY protocol clock. Similarly, the FlexCAN can also use the buffered crystal as a reference.

When a ferrite bead is used, it should have a low resistance at DC voltage with an increasing resistance at higher frequencies (100 MHz). The following table shows a recommended ferrite bead.

Table 13. Recommended ferrite bead

Manufacturer	Part number	DC resistance	Impedance at 100 Mhz, 20°C	Rated current	Package size	Operating temperature range
Murata	BLM31PG391SN1	0.05Ω	390Ω ±25%	2000[1] mA	1206	-55 to +125°C

1. 1000 mA at 125°C

4 Power supply requirements

The MPC5500 devices require 5V, 3.3V, and 1.5V power supplies. The 1.5V can be generated using an on-chip regulator controller with a linear external pass transistor.

The table below lists the supplies required by the MPC5500. Many of the supply pins can be used over a wide voltage range. Low voltage supplies generally can be used at nominal voltage ranges from 1.8 to 3.3 V and high voltage supplies can use a nominal 3.3 or 5 V supply. There are several supplies that must be a particular voltage (either 3.3 V or 5 V). The simplest board configuration uses 3.3 V and 5 V as the main external supplies and uses the internal 1.5 V regulator controller. The most commonly used configuration uses a bus voltage of 3.3 V and all peripheral I/O modules at 5.0 V. Due to power supply segmenting, some peripheral power supplies can be used at 3.3 V and some at 5 V if required, as long as the pins are on different power supply segments. The I/O voltage is the same for all pins sharing a common power supply segment. In addition, if standby SRAM operation is required (SRAM is kept powered while all of the other supplies are off), a 1.0 V SRAM standby supply should be provided.

Table 14. MPC5500 power supply requirements

Symbol	Description	Voltage range[1]	Maximum current[2]
VDDE_H	External I/O Supply Input	3.3V-5.0V	40 mA[3]
VPP	Flash program/erase supply input	5.0V	35 mA
VDDA	Analog power input	5.0V	25 mA
VDDE, VDD33, VDDSYN	External "low" voltage I/O supply input	1.8V-3.3V	15 mA
VRC33	Voltage Regulator Control supply	3.3V	320 mA
VFLASH	Flash read supply input	3.3V	4 mA

Table continues on the next page...

Table 14. MPC5500 power supply requirements (continued)

Symbol	Description	Voltage range[1]	Maximum current[2]
VDD	Internal logic supply input	1.5V	450 - 875 mA[4]
VSTBY	SRAM standby power input	1.0	<300µA[5]

1. Nominal voltage
2. Consult the electrical specifications in the device Data Sheet for the latest specifications.
3. I/O current required for driving external loads are not included. See the device Data Sheet for calculating required based on the load and switching frequency.
4. Maximum current depends on the device. See the individual device data sheet.
5. At the maximum specified device junction temperature of 150°C.

4.1 Internal regulator control, VDD, bypassing

The MPC5500 MCUs contain an internal regulator control circuit for the 1.5 V internal core supply. The control circuit requires an external pass transistor. The recommended pass transistor for the internal regulator is the On Semiconductor BCP68T1 NPN medium power transistor.

NOTE

The BCP68 transistor requires more heat-sinking than the minimum SOT223 footprint board layout. Extra area is required.

An alternate transistor is the On Semiconductor NJD2873T4G[7]. This transistor is in a DPAK package and allows for higher power dissipation. The NJD2873T4G is recommended for the MPC5554, MPC5561, and MPC5566. All of the other devices in the MPC5500 family can use the BCP68.

Table 15. Pass transistor requirements

Symbol	Description	Value	Unit
h_{FE}	DC current gain	> 85[1]	—
P_D	Power Dissipation	> 1.0[2]	Watts
I_C	Collector current (maximum)	1.0	A

1. The maximum gain should be less than 550.
2. 1.5W preferred

The table below shows the recommended pass transistors for the different MPC5500 devices.

Table 16. Recommended pass transistors by device

Device	Recommended pass transistor
MPC5534	BCP68 or NJD2873T4G
MPC5553	BCP68 or NJD2873T4G
MPC5554	NJD2873T4G
MPC5561	NJD2873T4G
MPC5565	BCP68 or NJD2873T4G

Table continues on the next page...

7. Also available from On Semiconductor is the MJVNJD2873T4G that provides full Automotive AEC-Q101 qualification and Unique Site and Control Change requirements.

Table 16. Recommended pass transistors by device (continued)

Device	Recommended pass transistor
MPC5566	NJD2873T4G
MPC5567	BCP68 or NJD2873T4G

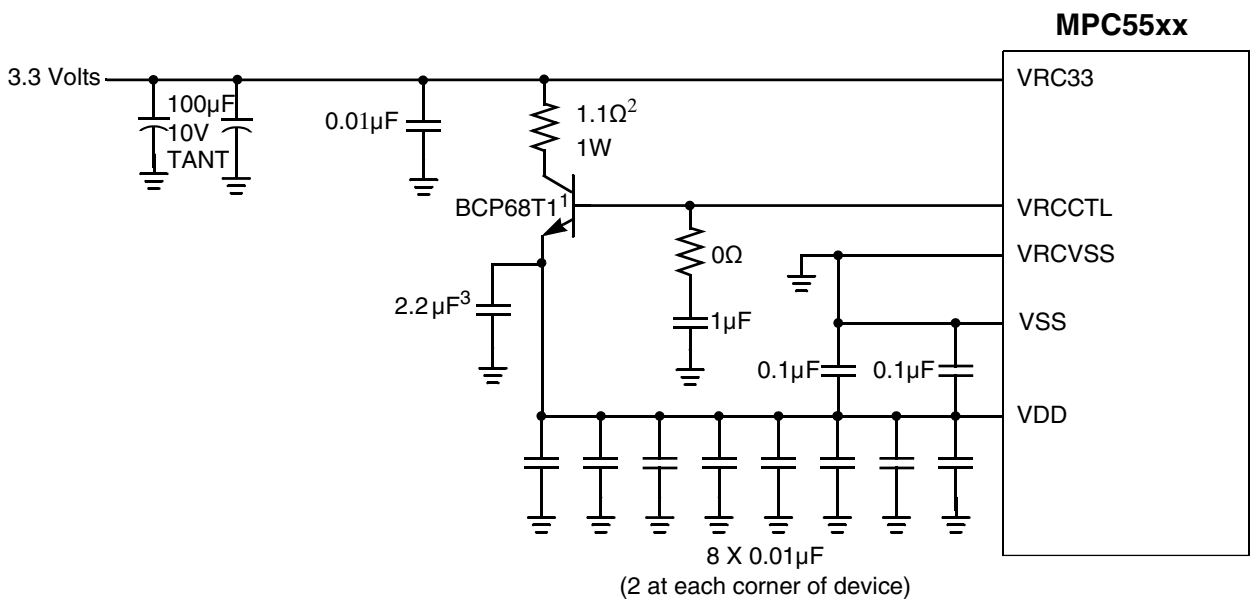
When using the on-chip 1.5-V regulator, the following bypass capacitors should be used on the VDD pins: one 2.2µF, two 100nF, and eight 10nF capacitors. These should be the only bypass capacitors on the VDD supply pins. A higher value collector bulk capacitor may be required in some board layouts to reduce regulator oscillation. Board layouts should accommodate the option of a base resistor and allow for a collector capacitor in the range of 1 to 22 µF.

Table 17. VDD bypass capacitors

Quantity	Value
1	2.2 µF
2	100 nF
8	10 nF

The 2.2 µF capacitor should be located near the emitter of the NPN transistor. The 10 nF should be placed as close as possible to the device pins.

The following figure shows the recommended configuration of the internal 1.5 V regulator controller, including the recommended bypass capacitors.



Notes:
1. Alternate pass transistor NJD2873T4. The NJD2873T4 does not require a collector resistor.
2. Power dissipation resistor (size 2512, 1 Watt).
3. This bulk capacitor should be near the emitter of the BCP68T1/NJT2873T4.

Figure 11. MPC5500 internal regulator supply connections

4.2 VDDSYN considerations

VDDSYN is the power supply for the oscillator and the clock Frequency Modulated Phase Lock Loop (FMPLL or PLL for short). VDDSYN should be filtered separately from the rest of the 3.3 V power supplies to reduce both noise on the main 3.3 V supply and to prevent noise from the 3.3 V supply affecting the stability of the PLL.

4.3 External memory power requirements

If external memories are included in the final system, the currents need to be provided from the system power supply. The maximum currents for the SRAM devices included in this application note are shown in the following table.

Table 18. External memory power requirements

Memory	Part number	Voltage (V)	Maximum Current (mA)
Cypress SRAM	CY7C1338	3.3V	375 mA
ISSI SRAM	IS61SF12832	3.3V	280 mA
ISSI SRAM	IS61SF25618	3.3V	170 mA

4.4 Decoupling capacitors

Local decoupling capacitors should be used on every MCU power supply pin. Many of the capacitors can be mounted on the underside of the PCB and should be located as close as possible to the respective power pins. In addition to the MCU, all other IC devices should have decoupling capacitors close to each power supply pin. Although not used on the MPC5500 evaluation boards, Dupont™ has developed an embedded capacitor board process that uses the entire power and ground places of the PCB for capacitors. This uses their Interra™ HK 10 planar capacitor laminate (approximately 2nF per square inch) and could be used to eliminate some of the localized bypass capacitors[8]. See AN2705 "Signal Integrity Considerations with MPC5500-based systems" and AN2706 "EMC Guidelines for MPC5500-based Systems" for more information on bypass capacitors for the power supplies.

4.5 Enhanced Queued Analog to Digital Converter supply connections

The enhanced Queued Analog to Digital Converter (eQADC) should use a filtered power supply separate from the digital 5V. On the MPC5500 evaluation boards, a separate 5 V supply is used as a separate filtered analog supply for the eQADC. Filtered reference supplies should be provided for high and low voltage references (VRH and VRL). The impedance of the traces of the following analog differential pairs should be matched: AN0/AN1, AN2/AN3, AN4/AN5 and AD6/AN7.

Unused Analog inputs should be pulled to ground.

The following figure shows the proper connections of the eQADC power supply connections.For best noise performance, the voltage reference high and low pins (VRH, VRL) should be filtered and kept clean.

8. Due to cost, these typically are not used in Automotive applications, but is mentioned for other types of applications that may need a reduced set of external components.

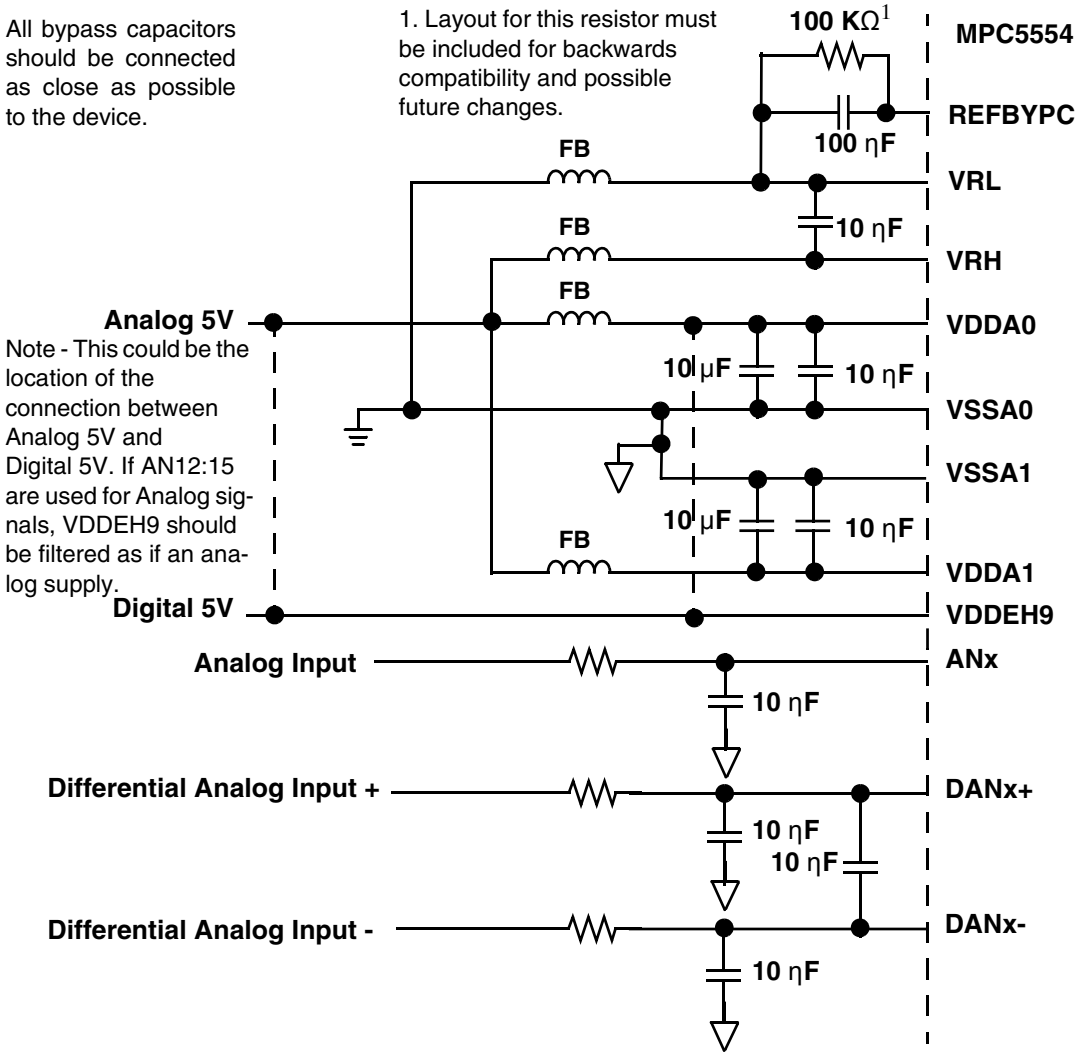


Figure 12. MPC5500 Preferred eQADC supply bypassing

4.6 Miscellaneous power requirements

Additional board components also require current from the supplies. The power supply should be designed to support the current requirements of all external devices. The table below shows the maximum current ratings for the major contributing devices (in addition to the MPC5500 MCU and the external SRAM).

Table 19. External device power requirements

Device	Part Number	Nominal Voltage (V)	Maximum current (mA)
Ethernet Physical Interface	DP83848	3.3V	375 mA
LIN Transceiver	MC33661	12V	8 mA
CAN Transceiver	TJA1050T	5V	75 mA
FlexRAY transceiver	TJA1080AT	3.3V - 5V	62 mA
RS232 Transceiver	HIN202	5V	15 mA

5 External pull resistors

Except in the cases documented in this application note, external pull up or down resistors are not required on any pins, except to over ride the default state of the pins. After reset, the state of the pull device is controlled by the pad configuration register in the System Integration Unit (SIU_PCR0–SIU_PCR230) for that pin. The direction of the internal pull device is documented in the device Data Sheet and Reference Manual, however, the setting can be changed by software in the PCR register for each pin.

5.1 Bus control pins

Unless the MPC5500 device is not in multi-processor mode (BOOTCFG[0:1] = 0b11, $\overline{\text{RSTCFG}}$ = 0b0), the bus control pins are not enabled. This allows minimum configuration boards to eliminate pull up resistors on the Bus request ($\overline{\text{BR}}$), Bus Grant ($\overline{\text{BG}}$), and Bus Busy ($\overline{\text{BB}}$) pins. Normally, external pull ups are not required on the Transfer Acknowledge ($\overline{\text{TA}}$) and Transfer Error Acknowledge ($\overline{\text{TEA}}$) signals, but pull ups have been included on the MPC5500 evaluation board to handle situations where they might be required.

5.2 Timer pins

Following reset, all of the enhanced Modular Input/Output System (eMIOS) and enhanced Timing Processor Unit (eTPU) pins have a default state based on the WKPCFG pin. If WKPCFG is high, then the timer pins have pull ups and pull downs if WKPCFG is low. If the state of some of these pins needs to be over-ridden during reset, an external pull is required that has a value strong enough to overcome the internal 130µA pull current. WKPCFG is latched 4 clocks prior to the negation of $\overline{\text{RSTOUT}}$ by the MCU.

5.3 Other pins

To ensure that the internal factory test modes are not entered accidentally, a strong pull up (1-2KΩ) can be placed on the TEST pin to VDDE7 (usually 3.3 V). This is the same power supply as the Nexus pins. Unused pins should be configured with both the input and the output buffers turned off, but with the weak pull downs enabled.

6 External bus interface

The MPC5500 devices in most packages include a 32-bit wide external data bus with up to a 26-bit address bus. On some devices, however, the package limits the data bus to only 16-bits and in other cases, does not support any access to an external data or address bus. An address bus of 20-bits is supported on all devices that support an external bus, however, some devices support an address bus of up to 24-bits and in some cases 26-bit, for the external address bus. On the Freescale evaluation boards, the external bus is used for access to SRAM only. The external bus could also be connected to a variety of other devices, such as stand-alone Flash memories or peripherals (either fast or slow[9]). When using the Ethernet interface on the MPC5553 and MPC5566 on the MPC5553 evaluation board, only a 16-bit data bus is available. The MPC5534 and MPC5565 always have only a 16-bit data bus. The address bus width for the different devices in the MPC5500 family is shown in the following table.

9. Keep in mind, however, that accesses to the external bus stalls the core CPU any time data is read from the external bus.

Table 20. Address bus width support

Device	Maximum Address bus signals	External Address signals available[1]
MPC5534	24-bit	ADDR[8:31]
MPC5553	24-bit	ADDR[8:31]
MPC5554	24-bit	ADDR[8:31]
MPC5561	26-bit	ADDR[12:31], ADDR[8:31], or ADDR[6:29]
MPC5565	26-bit	ADDR[10:31][3]
MPC5566	26-bit	ADDR[12:31], ADDR[8:31], or ADDR[6:29]
MPC5567	26-bit	ADDR[12:31], ADDR[8:31], or ADDR[6:29][2]

1. The number of address signals may depend on the package size. All ADDR signals may not be available on pins.
2. ADDR[10:31] in the 324 PBGA package.
3. Limited by package.

NOTE

ADDR[31] is the least significant bit of the MCU external address. Depending on the memory size (by-32, by-16, or by-8), ADDR[29], ADDR[30], or ADDR[31] may be connected to the least significant address line of the memory (ADDR0).

NOTE

Likewise, on memories that require the data bus (DATA) be connected in a particular order (primarily external Flash memories that require programming via specific data bus access values), DATA[31] is the least significant bit of the data and DATA[0] is the most significant bit of the data.

Some devices support a separate Calibration Bus Interface that is independent from the External Bus Interface. This document does not cover use of the calibration bus interface. On the MPC5500 MCUs, the Calibration Bus Interface is 16-bit data bus. The address bus can be from 19 to 21 bits depending on the number of chip selects required. The Calibration Bus is only available in a special "VertiCal" package. The VertiCal package fits in the same footprint (a small additional footprint is required for alignment keys) as the standard production device. See the VertiCal documentation for each device. The following table shows the calibration bus configurations available on the MPC5500 devices.

Table 21. Calibration Bus Support

MCU	Calibration Bus Interface supported
MPC5534	Yes (ADDR[10:30])
MPC5553	Partial[1]
MPC5554	No
MPC5561	No
MPC5565	Yes (ADDR[10:30])
MPC5566	Yes (ADDR[10:30])
MPC5567	Yes (ADDR[10:30])

1. ADDR[12:26] are shared with the normal external address bus interface signals. ADDR[10:11] and ADDR[27:30] are separate calibration bus signals. Calibration data bus uses the External Bus Interface DATA[16:31]. See appendix B "Calibration" of the MPC5553/MPC5554 Microcontroller Reference Manual.

6.1 External SRAM

The MPC5500 evaluation boards provide 512 KB of SRAM (either 256K by 16 or 128K by 32) that can be used for calibration overlay or program development. Only CS0 and CS1 are available on the evaluation boards for the SRAM chip select, however, in target systems, any chip select pin could be used. The IS61SF25618/IS61SF12832-10TQI (ISSI) is the preferred SRAM; however, the Cypress CY7C1338 is pin compatible. An access time of 10 nS is sufficient for the MPC5500 devices since the external bus runs at 1/2 the system frequency of 132 MHz (66 MHz bus maximum). The by-18 device is recommended instead of the by-16 since it seems to be more widely available. The following table shows suggested SRAMs.

Table 22. Example SRAM part numbers

Manufacturer	Part number	Size	Supply Voltage	Speed	Burst	Temperature range	Comments
ISSI	61SF12832-10TQI	4 Mbit (128k x 32)	3.3V[1]	100 MHz	Yes	Industrial	Pin compatible to Cypress
ISSI	61SF25618-10TQI	4 Mbit (256k x 18)	3.3V[2]	100 MHz	Yes	Industrial	
Cypress	CY7C1338	4 Mbit (128k x 32)	3.3/2.6V	100 MHz	Yes	Industrial	Flow through SRAM

1. 2.6V version available, 61SLF12832-10TQI
2. 2.6V version available, 61SLF25618-10TQI

All of the listed SRAMs are burstable, flow-through (non-pipelined) devices that operate in 32-bit mode and can also be addressed as bytes or half-words. This is preferable over the CY7C1339 as it allows better emulation of different wait states for benchmarking and flash emulation. The CY7C1339 is a pipelined access and requires a minimum of 1 wait state, regardless of the operating speed.

The figure below shows a typical 32-bit SRAM interface. For a 32-bit bus, address lines ADDR[30] and ADDR[31] may not need to be connected to the memory if byte selection uses the WE/BE enables. If two by-16 memories are connected to form a 32-bit data patch, ADDR[30] selects which 16-bit memory will be selected.

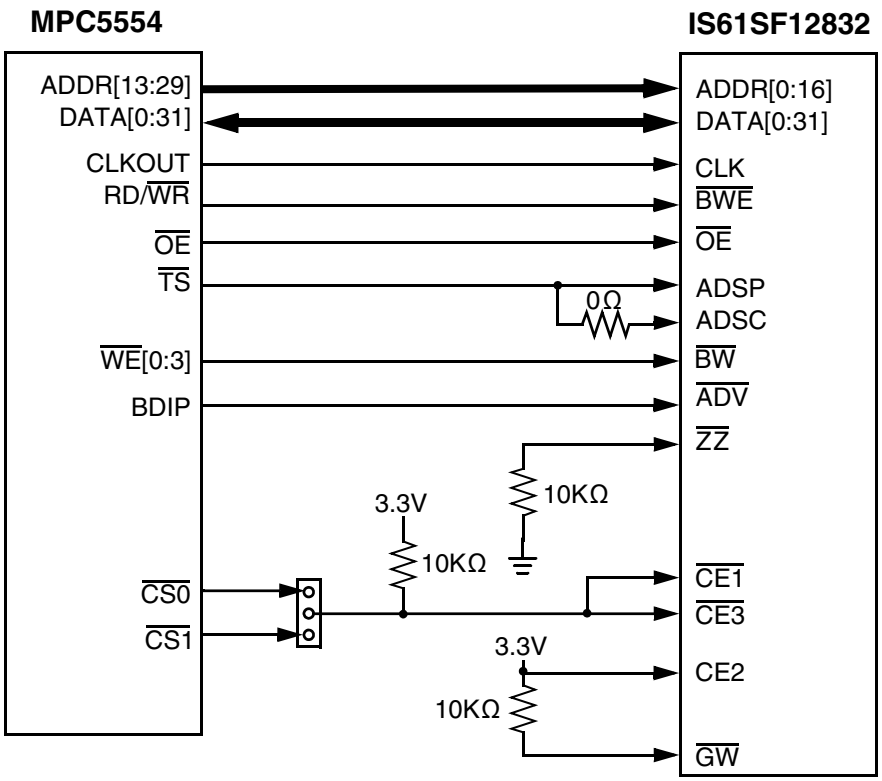


Figure 13. MPC5554 to ISSI 61SF12832 interface (32-bit bus)

The figure below shows a typical 16-bit SRAM interface. Connection of ADDR31 may not be required for 16-bit memories that use WE[0:1] to select between bytes of the 16-bit word.

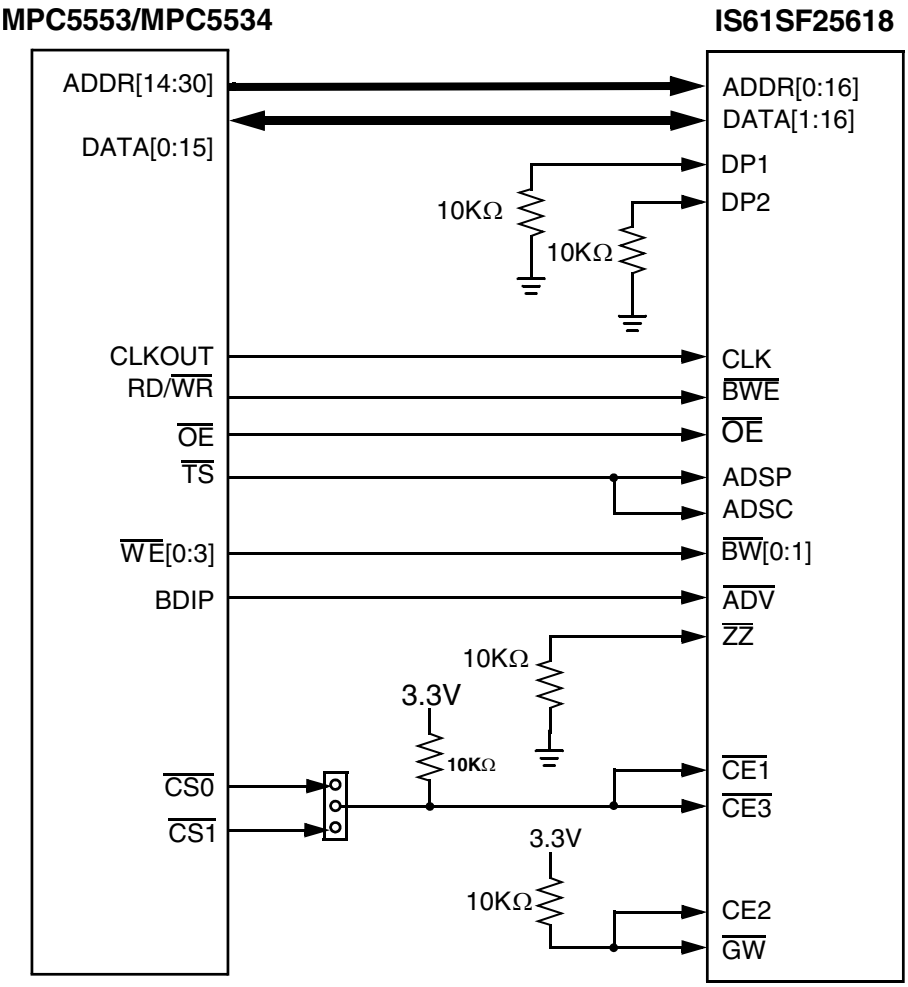


Figure 14. MPC5534 to ISSI 61SF25618 SRAM interface

Many memory devices allow the data bus to be connected as required for the best board routing, however, it is extremely important to ensure that the proper Write Enable/Byte Enable[10] pins are connected with the proper bytes of the data bus pins. Many SRAM devices name each byte of the data bus DATAa and do not number the actual SRAM bits. The associated Write Enable would also be WEa. The following table shows the mapping of the Data bus pin to write enable pin for the data bus.

Table 23. Data Bus to Write Enable/Byte Enable (WE/BE) mapping

Data Bus Pins	Write Enable/Byte Enable
DATA[0:7]	WE[0]
DATA[8:15]	WE[1]
DATA[16:23]	WE[2]
DATA[24:31]	WE[3]

Asynchronous SRAMs may also be used, but are not covered in this application note.

10. Selection of whether the WE[0:3]/BE[0:3] pins act as a Write Enable or a Byte Enable is controlled by a bit in the Memory Controller control registers and is settable on a chip select basis.

6.2 External bus termination

High speed signals should either be terminated or laid out with a fixed impedance of approximately 33Ω. On the MPC5500 evaluation boards, only the Clock Out (CLKOUT) pin is terminated. CLKOUT runs in two directions on the evaluation board, through a series terminating resistor (in a very short trace to the SRAM) and is fully terminated at the end of the trace that runs to the Nexus connectors. The Engineering Clock (ENGCLK) has series termination only.

7 Nexus Connector Recommendation and Pin-Out Definitions

For the MPC5500 family, Freescale recommends that a single 38-pin MICTOR connector be used on all boards for both reduced- and full-port Nexus modes (M38C). In cases where a more robust connector is required, Freescale recommends that the 51-pin Glenair connector be used (R51C).

The table below shows the possible connectors that can be used for the MPC5500 family devices.

Table 24. Recommended Nexus Connectors for the MPC5500 Family

Connector	Designation	Part number (for target system)	Total number of pins	Maximum message data out signals (per Nexus standard)
3M MICTOR	M38C	767054-1	38 (+ 5)	8 (12 by extension)
3M MICTOR	M38-2C	767054-1[1] X 2	76 (+ 10)	16
Glenair MicroD Robust	R51C	MR7580-51P2BNU	51	8 (12 by extension)[2]

1. Other compatible part numbers are 2-5767004-2 (RoHS compliant), 2-767004-2, 767061-1, and 767044-1.
2. Although the Nexus standard definition normally only allows eight MDO signals, Freescale has extended the definition to include an extra four MDO signals.

Since full-port mode requires twelve MDO pins and both of these connectors[11] support only eight MDO pins, Freescale redefined some of the of the Vendor_IO and Tool_IO pins for the additional MDO signals (MDO[8:11]) on the MPC5500 family devices. The MICTOR connector option in the Nexus standard defined five vendor-defined pins (Freescale uses four of these signals for the extra MDO signals and left one extra pin), but the 51-pin robust connector only has three Vendor_IO pins. Therefore, to support the full twelve MDO signals, two Tool_IO pins were also defined as MDO signals on the robust connector option. The table below shows the recommended signal usage for the vendor-defined I/O pins, as well as tool vendor-defined I/O pins. Freescale has worked with tool vendors to ensure minimal impact to tool needs on these pins.

Table 25. Extended MDO definition to the Nexus Standard Connector using IO for additional MDO Signals

Nexus pin designation	MPC5500 MICTOR definition	MPC5500 robust definition
VEN_IO0	MDO9/GPIO80	MDO9/GPIO80
VEN_IO1	MDO11/GPIO82	MDO11/GPIO82
VEN_IO2	BOOTCFG1/$\overline{\text{IRQ3}}$/GPIO212	$\overline{\text{RSTOUT}}$[1]
VEN_IO3	MDO8/GPIO70	—[2]
VEN_IO4	MDO10/GPIO81	—
TOOL_IO0	-[3]	—
TOOL_IO1	—	—

Table continues on the next page...

11. per the IEEE-ISTO 5001-2003 "Nexus" standard

Table 25. Extended MDO definition to the Nexus Standard Connector using IO for additional MDO Signals (continued)

Nexus pin designation	MPC5500 MICTOR definition	MPC5500 robust definition
TOOL_IO2	—	MDO8/GPIO70
TOOL_IO3	RSTOUT	MDO10/GPIO81

1. This pin has been redefined since the original definition in 2004. Customers may want to make this signal selectable (via a 0 Ω resistor option) between RSTOUT and BOOTCFG1/IRQ3/GPIO212.
2. This signal is not available on the 51-pin robust connector
3. This pin is defined for use by tool vendors and has no defined connection to the MPC5500 device for the MICTOR connector option.

7.1 MICTOR Connector Definition for the MPC5500 Family

The following table shows the complete signal usage for the MPC5500 full-port mode MICTOR connector. This uses the Vendor_IO pins 1–4 as MDO[11:8]. This connector may also be used for reduced-port mode (which only uses MDO[3:0]). While only one MICTOR connector is recommended, some tools may not support this configuration. For maximum tool compatibility, a second MICTOR connector may need to be added for the upper four MDO signals (MDO[11:8]).

Table 26. MPC5500 Family MICTOR Connector M38C

MPC5500 signal	Combined M38C or M38-2C						Combined M38C or M38-2C	MPC5500 signal
-	Reserved	-	1	Ground	2	-	Reserved[1]	-
-	Reserved[1]	-	3		4	-	Reserved[1]	-
MDO9/GPIO80	VEN_IO0	Out	5		6	Out	CLOCKOUT	CLKOUT
BOOTCFG1/IRQ3/ GPIO212	VEN_IO2	In	7		8	Out	VEN_IO3	MDO8/GPIO70
RESET	/RESET	In	9		10	In	/EVTI	EVTI
TDO	TDO	Out	11		12		VTREF	VDDE7
MDO10/GPIO81	VEN_IO4	Out	13		14	Out	/RDY	RDY
TCK	TCK	In	15		16	Out	MDO7	MDO7/GPIO78
TMS	TMS	In	17	Ground	18	Out	MDO6	MDO6/GPIO77
TDI	TDI		19		20	Out	MDO5	MDO5/GPIO76
JCOMP	/TRST	In	21		22	Out	MDO4	MDO4/GPIO75
MDO11/GPIO82	VEN_IO1	Out	23	Ground	24	Out	MDO3	MDO3
RSTOUT	TOOL_IO3	Out	25		26	Out	MDO2	MDO2
-	TOOL_IO2		27		28	Out	MDO1	MDO1
-[2]	TOOL_IO1		29		30	Out	MDO0	MDO0
12 volts	UBATT		31		32	Out	/EVTO	EVTO
12 volts	UBATT		33		34	Out	MCKO	MCKO
-[2]	TOOL_IO0		35		36	Out	/MSEO1	MSEO1
VSTBY	VALTREF		37		38	Out	/MSEO0	MSEO0

1. Pins 1 through 4 should be considered "reserved" and may be used by some logic analyzers as ground connections. If care is taken (and the proper cables are used), these pins could be used for customer I/O signals. However, check with the tool vendors used. These pins are defined on devices that require 16 MDO signals.
2. This optional Nexus signal is defined for use by tool vendors and has no defined connection to the MPC5500 family device.

7.2 MPC5500 JTAG connector

The figure below shows the pin-out of the recommended JTAG connector to support the MPC5500 devices. If there is enough room allowed in the target system, a full Nexus connector is preferred over the simple 14-pin JTAG connector since it allows a higher degree of debug capability. It can be used as a minimum debug access or for BSDL board testing.

The recommended connector for the target system is the Tyco part number 2514-6002UB and the pin-out is shown in the following table.

NOTE

This pin-out is similar to the Freescale MCORE and DSP JTAG/OnCE connector definitions.

Table 27. Recommended JTAG connector pinout

Description	Pin	Pin	Description
TDI	1	2	GND
TDO	3	4	GND
TCK	5	6	GND
$\overline{\text{EVTI}}$[1]	7	8	—
$\overline{\text{RESET}}$	9	10	TMS
VREF	11	12	GND
$\overline{\text{RDY}}$[2]	13	14	JCOMP

1. $\overline{\text{EVTI}}$ is optional and was not included in the original (very early) definitions of the JTAG-only connector.
2. The $\overline{\text{RDY}}$ signal is not available on all packages or on all devices. Check the device pinout specification. In general it is not available in packages with 208 signals or less.

NOTE

Freescale recommends that a full Nexus connector be used for all tool debug connections, regardless of whether Nexus trace information is needed. Adapters for a JTAG class 1 14-pin connector (tool side) to the full Nexus MICTOR connectors (board side) are available from P&E Microcomputer Systems (http://www.pemicro.com), part number PE1906, and from Lauterbach (http://www.lauterbach.com), order number LA-3723 (CON-JTAG14-MICTOR). Lauterbach also has an adapter that will connect a MICTOR connector (tool side) to a 14-pin JTAG connector (board side). This adapter is order number LA-3725 (CON-MIC38-J14-5500).

7.3 Minimum debug external circuitry

In general, other than the connector, no additional circuitry is required for the Nexus/JTAG debug circuitry. The MPC5500 devices include internal pull devices that ensure the pins remain in a safe state. However, if there is additional circuitry connected to the Nexus/JTAG pins, or the signals have long traces, a minimum number of external pull resistors can be added to ensure proper operation under all conditions. Long traces could be affected by other signals, due to crosstalk from high-current or high-speed signals. The recommended external resistors are shown in the following table.

Table 28. Optional minimum debug port external resistors

Nexus/JTAG signal	Resistor direction and value	Description
JCOMP	10 kΩ pulldown	Holds debug port in reset and prevents any debug commands from interfering with the normal operation of the MCU.
$\overline{\text{RESET}}$	4.7 kΩ pullup	The $\overline{\text{RESET}}$ input should be driven from an open collector output; therefore, it requires a pull-up resistor for the MCU.
TD/WDT[1]	10 kΩ pulldown	With no tool attached, this signal should be held low and may or may not be connected to a pin of the MCU, depending on the system definition.
$\overline{\text{EVTI}}$	10 kΩ pullup	A pull-up resistor prevents debug mode from being forced after reset if debug mode is enabled (JCOMP = high). It also prevents breakpoints from being forced if debug mode is enabled. **NOTE:** In almost all situations, a resistor is not required on this signal.
TCK	series isolation resistor	A termination resistor or an isolation (0Ω) resistor may be required in systems that use a debug connector on the VertiCal connector since the TCK signal may have multiple endpoints that can cause reflections.

1. This is an optional signal and is not actually required for the MCU.

In addition to the pull-up and pull-down resistors, some systems may want to use buffers between the Nexus/JTAG connector inputs and the MCU. This will prevent over-voltage conditions from causing damage to the MCU pins. Normal systems should not require this circuitry, but it is helpful in systems that can be exposed to improper connections that provide voltages that are outside the operating conditions of the MCU. A common circuit to use is the Texas Instruments SN74CBTLV3861[12]. This device is a bus switch that implements a bidirectional interface between two terminals with less than 5 Ω of resistance. It should be powered by the same supply that powers the debug port. The device enable should be connected to ground for the interface to be enabled whenever the debug port on the MCU is powered. This circuit provides a high impedance to the tool when the debug port is powered off.

NOTE

It is recommended that at least the reduced port configuration Nexus signals be made available (somewhere) on production boards. This facilitates debugging of new boards and analysis of errors in software, even on boards that have restricted space and normally provide a JTAG-only connection. If the Nexus signals are available on the production board, an adapter could be built to provide a Nexus connection on boards that do not have a complete footprint for one of the standard Nexus connectors. Likewise, the JTAG

12. SN74CBTLV3861-Q1 is automotive qualified if required.

connector does not have to be populated on production boards and could even utilize a smaller connector footprint that could be used with an adapter to the standard debug connections.

In systems that use a VertiCal mounted debug connector and have a JTAG connector/footprint in the target system, termination may be required on the JTAG Test Clock (TCK) to avoid ringing due to the multiple signal endpoints.

8 Example communication peripheral connections

There are a wide range of peripheral pins available on the MCUs. Many of these have fairly standard definitions for their use. This section provides example connections for some of the most commonly used communications peripherals, such as LIN, CAN, FlexRay, Ethernet, and RS-232 communication interfaces.

The table below summarizes the maximum communication speed and general overview information of the different types of interfaces.

Table 29. Communication module comparison

Common name	Standard	Distributed timebase	Speed (maximum Kbits/second)	Channels	Time triggered	Arbitration
RS-232D	EIA RS-232 revision D	No	115.2	Single	No	None (optional flow control)
K Line	ISO 9141	No	150[1]	Single	No	None
LIN	LIN 1.0, LIN 2.0, and LIN 2.1[2]	No	100[3]	Single	No	None (master/ slave)
CAN	Bosch 2.0B ISO11898	No	1,000[4]	Single	No (additional function)	CSMA[5]
FlexRay	FlexRay	Yes	10,000	Dual	Yes	TDMA[6]
Ethernet	IEEE® 802.3	No	10,000/100,000	Single	No	CSMA

1. Typical speed is 10.4Kbits/s.
2. Many Freescale devices only support the LIN 1.0 and 2.0 standards. LIN2.1 requires a different sampling scheme covered by an erratum to the LIN standard..
3. Typical speed is 10 or 20 Kbits/s, but supports a fast mode of 100 Kbits/s.
4. Two different speed classes are supported by CAN, a fast (250K to 1Mbits/s) and a low speed CAN (5K to 125Kbits/s).
5. Carrier Sense Multiple Access
6. Time Division Multiple Access

In a typical system, the battery reverse bias and over-voltage protection may be shared between all of the communication devices in the target system. The below figure shows a typical protection circuit.

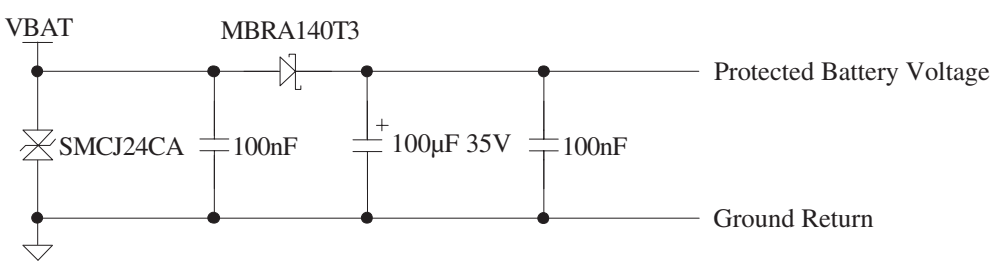


Figure 15. Typical protection circuit

8.1 Example RS-232 interface for eSCI

The RS-232 (TIA/EIA-232-F) standard is a fairly common interface that was once available on nearly all computers. While this interface is disappearing, adapters are available to allow the use of RS-232 peripherals though other interfaces, such as USB. RS-232 was intended to be a very low-cost, low-performance interface. This interface was originally specified with signal voltages of +12 V and -12 V typically. However, this has been lowered to a typical minimum voltage of +5 V and -5 V in recent years.

On many of the Freescale automotive MCUs, the enhanced Serial Communication Interface (eSCI) module implements the standard Universal Asynchronous Receiver/Transmitter (UART) functions. This same module (eSCI) also supports the Local Interconnect Network (LIN) interface (with a different physical layer device).

The figure below shows the typical connections between the serial port of an MCU and the MAX3232-EP RS-232D transceiver from Texas Instruments (http://www.ti.com/). The transceiver operates from either a 3.3 V or a 5 V supply and includes two charge pumps to generate the output voltages that are required. This device contains two transmit drivers and two receivers. The charge pumps require four external capacitors.

NOTE

The commercial grade MAX3232 device is not rated for the full automotive temperature range of -40 to +125° C and is not intended for automotive applications. This circuit should not be used or populated in a production module intended for automotive use. However, in many cases, the RS-232 interface is intended only as a development interface; therefore the commercial device can be used for prototyping purposes. TI does offer a device option with an operating temperature range of -40 to +85° C. TI has an enhanced version of the device, MAX3232-EP, which is intended for aerospace, medical, and defense applications. This version is available with an operating temperature range of -55 to +125° C.

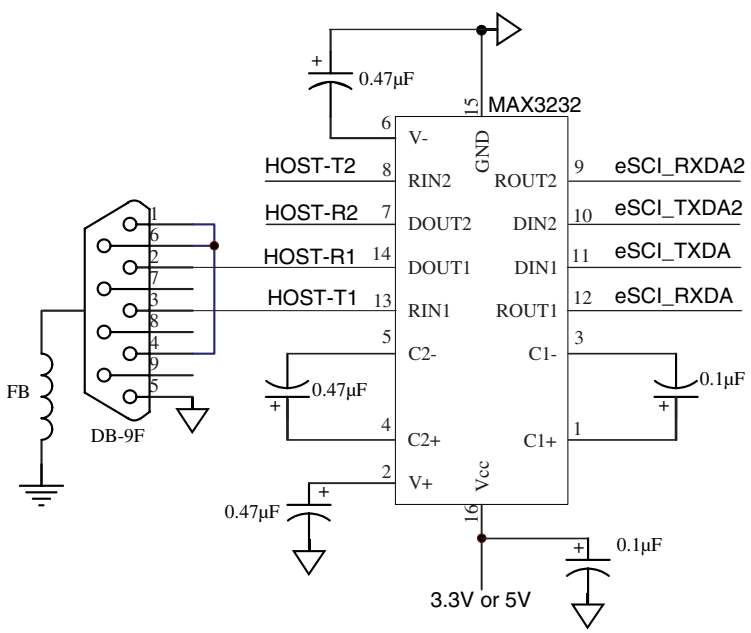


Figure 16. Typical eSCI to RS-232D circuit

The following table shows the standard connection of the RS-232 connector, as used on the Freescale evaluation boards.

Table 30. Typical RS-232D Connector Definition

6 Connect to pin 1 and 4	**1** Connect to pin 4 and 6
7 N/C	**2** RS-232 TX (Transmit)
8 N/C	**3** RS-232 RX (Receive)
9	**4** Connect to pin 1 and 6
	5 GND

NOTE

N/C pins are not connected.

Shell of connector should be connected through a ferrite bead to ground.

8.2 Example LIN interface for eSCI

Local Interconnect Network (LIN) is a commonly used low-speed network interface that consists of a master node communicating with multiple remote slave nodes. Only a single wire is required for communication and is commonly included in the vehicle wiring harness.

On many of the Freescale automotive MCUs, the enhanced Serial Communication Interface (eSCI) module implements Local Interconnect Network (LIN) interface. This same module (eSCI) also supports the standard Universal Asynchronous Receiver/Transmitter (UART) functions (with a different physical layer device).

The following figure shows a typical interface implemented using the Freescale MC33661 LIN transceiver.

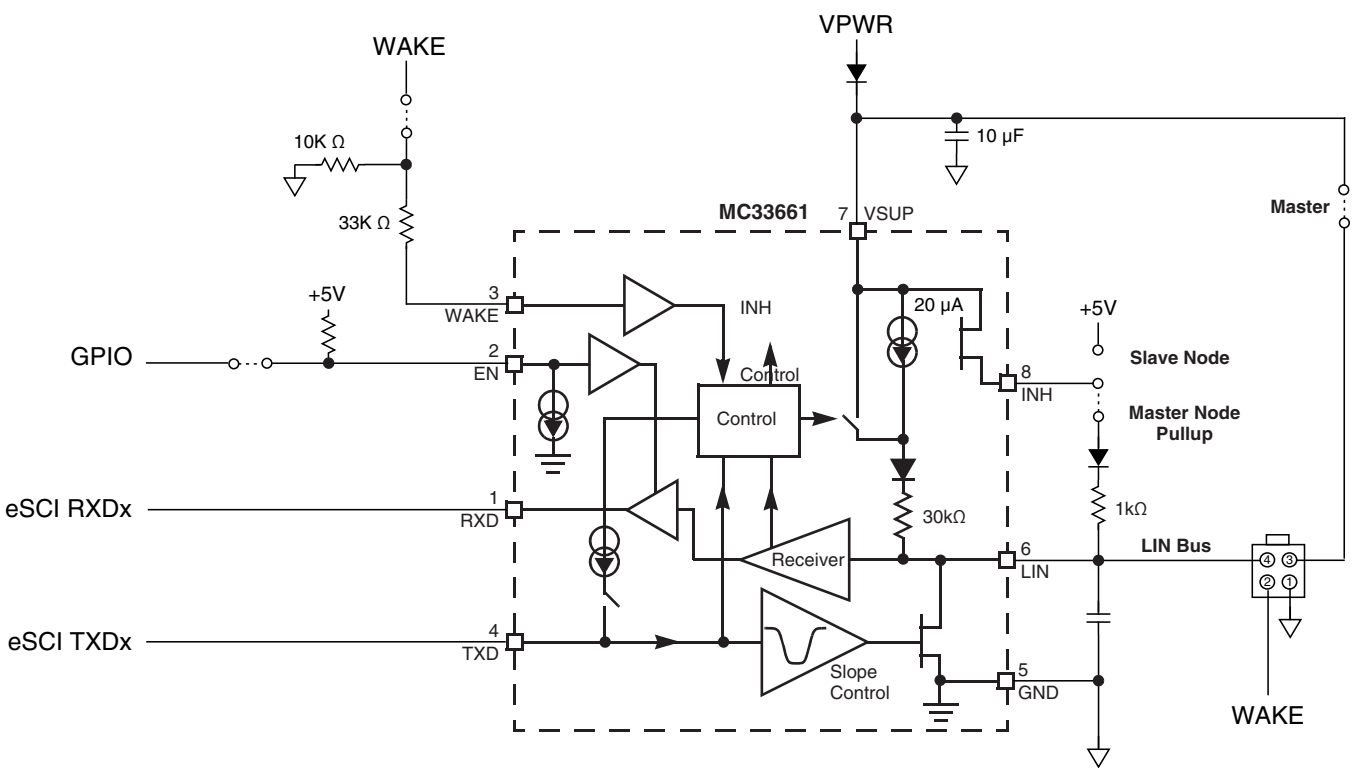


Figure 17. Typical eSCI to LIN connections

The table below shows the pins of the MC33661 and their typical connections to an MCU.

Table 31. MC33661 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	RXD	Output	Receive Data Output	MCU LIN RXD	LIN Receive Data Output to the MCU.
2	EN	Input	Enable Control	MCU GPIO	Enables operation of the device.
3	Wake	Input	Wake Input	LIN Bus Wake[1]	Wake enables the devices out of sleep mode.
4	TXD	Input	Transmit Data Input	MCU LIN TXD	LIN Transmit Data Input from the MCU.
5	GND	Input	Ground	System Ground Reference	Device ground reference.
6	LIN	Input/Output	LIN Bus	LIN bus	Bidirectional pin that represents the single-wire transmit and receiver.
7	VSUP	Input	Power Supply	Protected battery voltage	This is the power supply for the device and is typically connected to a nominal 12 V.
8	INH	Output	Inhibit Output	LIN Bus (if master)	The Inhibit pin controls either an external regulator to turn on a slave node or is connected through a resistor to the LIN bus on master nodes.

1. Wake is an optional signal on the LIN connector, but may come directly from a switch.

There is no standard industry-defined LIN connector. Freescale uses a 4-pin Molex that allows for the LIN bus pin, a power supply source (VPWR), a wakeup signal, and a ground reference. Slave nodes will often implement two connectors to allow a daisy-chain of multiple nodes to be easily implemented. The Freescale Molex connector definition is shown in the following table.

Table 32. LIN connector pin-out recommendation

Function	Pin number	Pin number	Function
LIN Bus	4	3	VPWR
Wake	2	1	Ground

In a typical system, these pins would be used as follows:

- LIN Bus - This is the single-wire LIN bus that connects between the master LIN node and the slave LIN nodes.

- VPWR - This connector input can be used as the power input to a slave node. Care should be taken that sufficient current is available for the total number of LIN slaves that are powered through this connection. In some systems, this may come from the master LIN node.
- Wake - The Wake signal is typically used for each individual slave node to enable the LIN physical interface of that node and consequently enable the power supply (using the INH output) to power up the MCU to perform some action. For example, when the handle on a car door is lifted, turn on the MCU that controls a function inside the vehicle, such as power a smart dome light or enable the controls of a smart seat.
- Ground - Ground reference for the module.

Part numbers for the 4-pin Molex Mini-Fit Jr.™ connector are shown in the table below.

Table 33. Recommended 4-pin Molex Mini-Fit Jr.™ connector part numbers

Description	Manufacturer part number (Molex)
4-pin right-angle connector with flange for target system, tin contacts, with latch	39-29-1048
4-pin right-angle connector with pegs for target system, tin contacts, with latch	39-30-1040
4-pin vertical connector with pegs for target system, tin contacts, with latch	39-29-9042
4-pin right-angle connector with flange for target system, gold contacts, latch	39-29-5043
Mating connector with latch for cable assemblies	39-01-2040
Female terminal for mating cable assembly	39-00-0077

8.3 CAN interface circuitry

Controller Area Network (CAN) is commonly used in almost all automotive applications to allow communication between various microchips in the car.

The number of CAN modules on-chip varies from device to device. A separate CAN transceiver is required for each CAN module, although some CAN transceivers may have more than one transceiver on a single chip. It is possible to connect two CAN modules to a single transceiver if the transmit pins are put into open-collector mode with an external pullup resistor. However, the value of this resistor may limit the maximum speed of the CAN module if not sized properly for the speed.

Freescale CAN modules conform to CAN protocol specification version 2.0B, and the transceivers shown in this application note comply with ISO 11898 physical layer standard.

Typically, CAN is used at either a low speed (5 kbit/s to 125 kbit/s) or a high speed (250 kbit/s to 1 Mbit/s). Powertrain applications typically use a high speed (HS) CAN interface to communicate between the engine control unit and the transmission control unit. Body and chassis applications typically use a low speed (LS) CAN interface. In the dashboard of a vehicle, there is typically a gateway device that interfaces between HS and LS CAN networks.

Freescale has a high-speed standalone CAN physical interface device with built-in diagnostic capabilities (MC33902), as well as CAN transceivers integrated with other functions[13]. Other popular CAN transceivers include the NXP devices shown in the following table. Example TJA1050 HS and TJA1054 LS circuits are shown in this application note.

Table 34. NXP CAN transceiver comparison

	TJA1050	TJA1054	TJA1040	TJA1041
Bitrate (kbit/s)	1000	125	1000	1000
Modes of operation	Normal, Listen-only	Normal, Standby, Sleep	Normal, Standby	Normal, Listen-only, Standby, Sleep

8.3.1 Recommended CAN connector

Generally DB-9 connectors are used for evaluation boards to connect CAN modules together, whereas there are various connectors used for production hardware. The following figure shows the DB-9 connector and socket configuration of a typical evaluation board connector. A socket (female) is used on the evaluation board and a cable with a connector (male) connects with it.

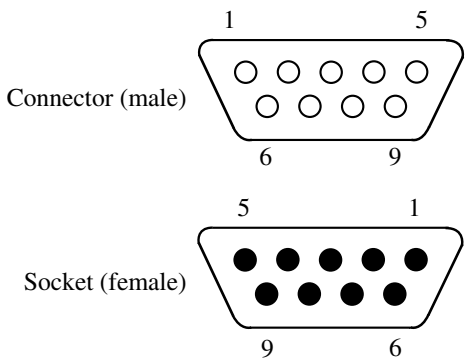


Figure 18. DB-9 connector and socket

The table below shows the typical connector pin-out definition.

Table 35. DB-9 pin signal mapping

Pin number	Signal name
1	N/C
2	CAN_L
3	GND
4	N/C
5	CAN_SHIELD (OPTIONAL)
6	GND
7	CAN_H
8	N/C
9	CAN_V+ (OPTIONAL)

13. An example device is the MC33905 that includes a 5 V power supply controller, a CAN transceiver physical interface, and a LIN transceiver physical interface.

NOTE

The metal shell of the socket should be connected through a ferrite bead to the chassis ground.

8.3.2 Low-speed CAN TJA1054 interface

The figure below shows the typical connections for the physical interface between the MCU and the CAN bus for low-speed applications using the NXP TJA1054 LS CAN transceiver. Optionally, the standby and enable pins can be connected to MCU GPIO pins for additional control of the physical interface.

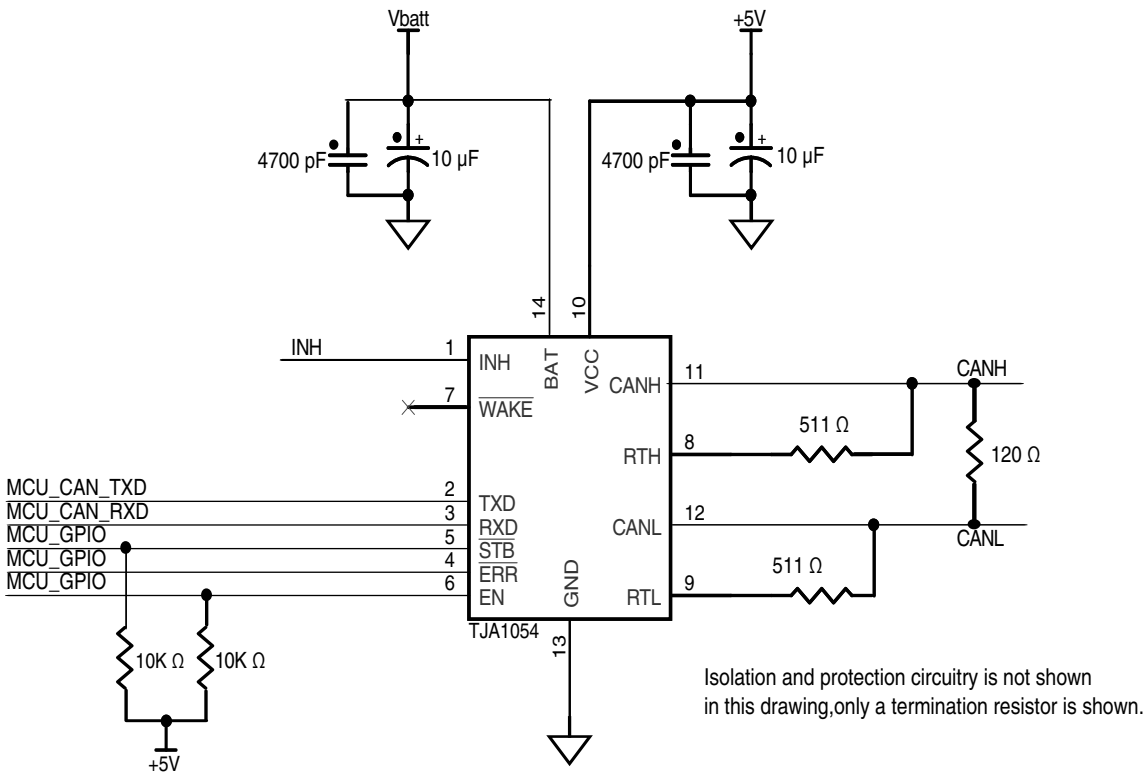


Figure 19. Typical low-speed CAN circuit using TJA1054

NOTE

Decoupling shown as an example only.

$\overline{\text{STB}}$ and EN should be pulled high for Normal mode. These signals can optionally be connected to MCU GPIO pins to allow MCU control of the physical interface.

The table below describes the TJA1054 pins and system connections.

Table 36. TJA1054 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	INH	Input	Inhibit	Typically not connected	Inhibit output for control of an external power supply regulator if a wake up occurs

Table continues on the next page...

Table 36. TJA1054 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
2	TXD	Input	Transmit Data	MCU CAN TXD	CAN transmit data input from the MCU
3	RXD	Output	Receive Data	MCU CAN RXD	CAN receive data output to the MCU
4	$\overline{\text{ERR}}$	Output	Error	MCU GPIO	The error signal indicates a bus failure in normal operating mode or a wake-up is detected in Standby or Sleep modes.
5	$\overline{\text{STB}}$	Input	Voltage Supply for IO	MCU GPIO	Standby input for device. It is also used in conjunction with the EN pin to determine the mode of the transceiver.
6	EN	Input	Enable	MCU GPIO	Enable input for the device. It is also used in conjunction with the STB pin to determine the mode of the transceiver.
7	$\overline{\text{WAKE}}$	Input	Wake	Typically not connected	Wake input (active low), both falling and rising edges are detected
8	RTH	Input	Termination Resistor High	Resistor to CANH	Termination resistor for the CAN bus high
9	RTL	Input	Termination Resistor Low	Resistor to CANL	Termination resistor for the CAN bus low[1]
10	VCC	Input	Voltage Supply	5 V	Digital IO supply voltage, 5 V
11	CANH	Output	CAN Bus High	CAN Bus Connector	CAN bus high pin
12	CANL	Input/Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin
13	Ground	Output	Ground	Ground	Ground return termination path
14	BAT	Input	Standby	Battery voltage	Battery supply pin, nominally 12 V

1. This allows the transceiver to control the CAN bus impedance under an error condition.

8.3.3 High-speed CAN TJA1050 interface

The figure below below shows the typical connections for the physical interface between the MCU and the CAN bus for high-speed applications using the NXP TJA1050 HS CAN transceiver.

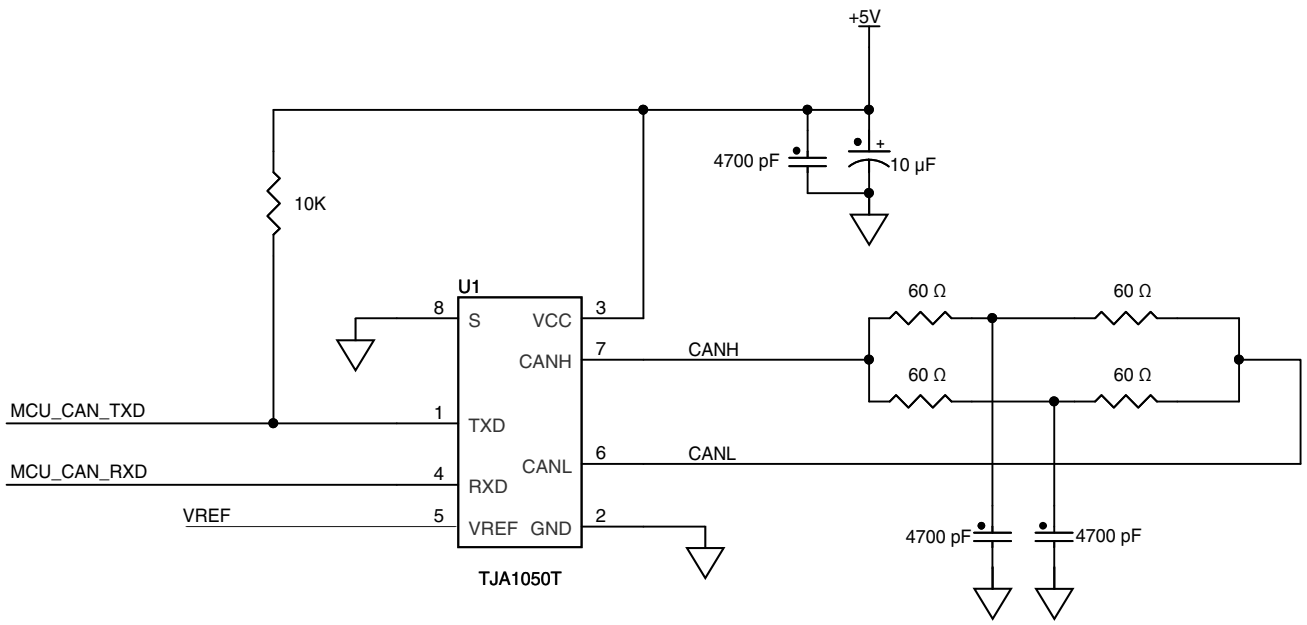


Figure 20. Typical high-speed CAN circuit using TJA1050

NOTE

Decoupling shown as an example only.

TXD/RXD pullup/pulldown may be required, depending on device implementation.

The table below as describes the TJA1050 pin and system connections.

Table 37. TJA1050 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	TXD	Input	Transmit Data	MCU CAN TXD	CAN transmit data input from the MCU
2	GND	Output	Ground	Ground	Ground return termination
3	VCC	Input	—	5 V	Voltage supply input (5 V)
4	RXD	Output	Receive Data	MCU CAN RXD	CAN receive data output to the MCU
5	VREF	Output	Reference voltage Output	Not used	Mid-supply output voltage. This is typically not used in many systems, but can be used if voltage translation needs to be done between the CAN transceiver and the MCU.
6	CANL	Input/Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin
7	CANH	Input/Output	CAN Bus High	CAN Bus Connector	CAN bus high pin
8	S	Input	Select	Grounded or MCU GPIO	Select for high-speed mode or silent mode. Silent mode disables the transmitter, but keeps the rest of the device active. This may be used in the case of an error condition.

8.3.4 High-speed CAN with diagnostics: MC33902 interface

For target systems that require full diagnostics of the CAN interface, the Freescale MC33902 high-speed CAN transceiver is available. Features of this device are:

- High-speed CAN interface for baud rates of 40 kbit/s to 1.0 Mbit/s
- Compatible with ISO 11898 standard
- Single supply from battery; no need for a 5.0 V supply for CAN interface
- I/O compatible from 2.75 V to 5.5 V via a dedicated input terminal (3.3 V or 5.0 V logic compatible)
- Low-power mode with remote CAN wakeup and local wake-up recognition and reporting
- CAN bus failure diagnostics and TXD/RXD pin monitoring, cold start detection, and wake-up sources reported through the ERR pin
- Enhanced diagnostics for bus, TXD, RXD, and supply pins available through pseudo-SPI via existing terminals EN, STBY, and ERR
- Split terminal for bus recessive level stabilization
- INH output to control external voltage regulator

A block diagram of this transceiver is shown below.

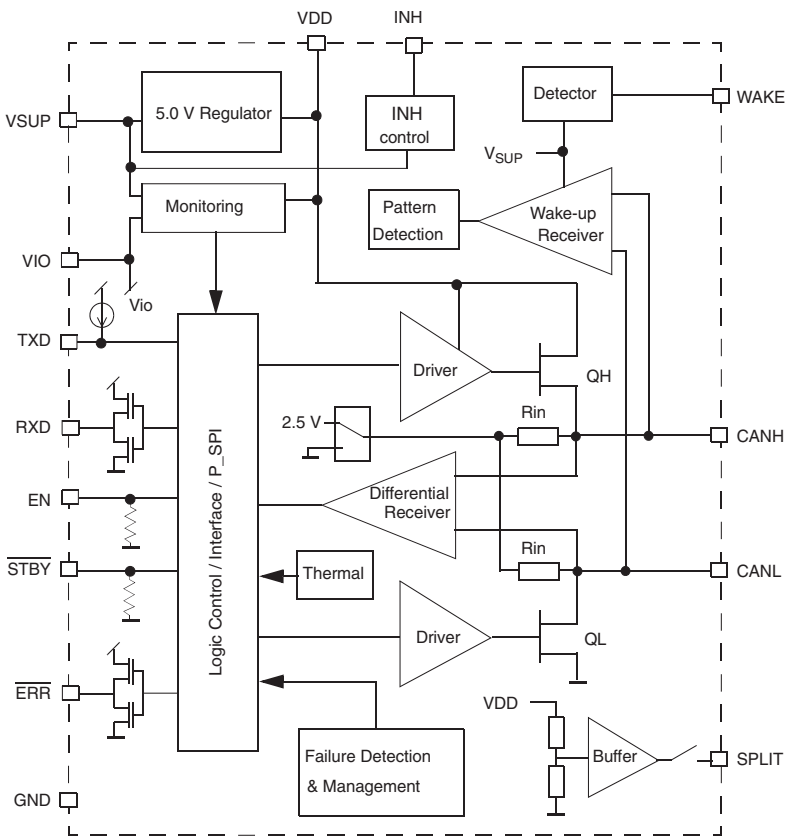


Figure 21. MC33902 block diagram

While a full SPI interface is not available for the diagnostic information, a quasi-SPI interface is available to communicate to the MCU. This interface is referred to as the P_SPI interface in the MC33902 data sheet.

The figure below shows an example schematic using the MC33902.

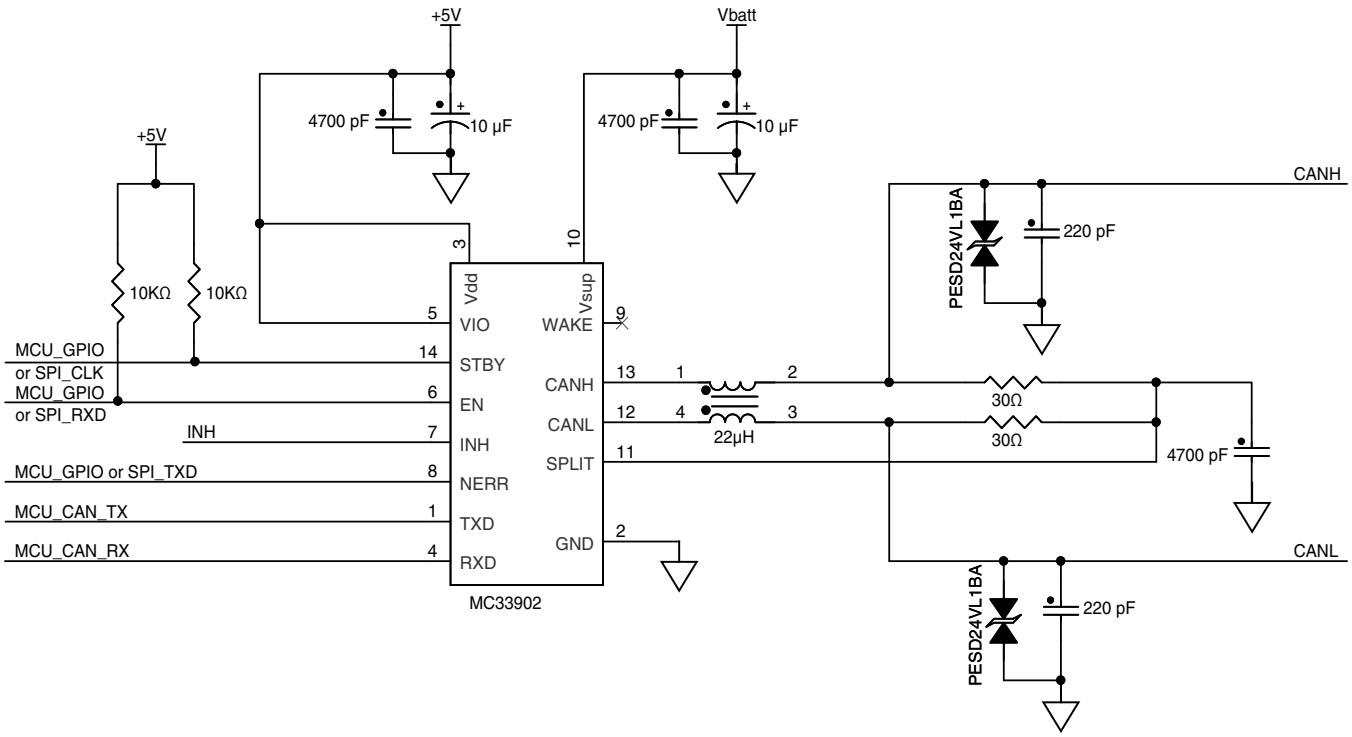


Figure 22. Typical high-speed CAN circuit using the MC33902

NOTE

Decoupling shown as an example only.

Bus protection is shown as an example only.

The table below shows the pins of the MC33902 and the possible connections to a MCU and the target system.

Table 38. MC33902 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	TXD	Input	Transmit Data	MCU CAN TXD	CAN transmit data input from the MCU
2	GND	Output	Ground	Ground	Ground termination
3	VDD	Output	VDD Internal Regulator Output	Bypass capacitors only	5 V power supply output. Requires external bypass capacitors.
4	RXD	Output	Receive Data	MCU CAN TXD	CAN receive data output to the MCU
5	VIO	Input	Voltage Supply for IO	3.3 V or 5 V	Supply voltage input for the digital input and output pins. This should be matched to the IO voltage supply of the MCU. Most typically, this is 5 V, but could also be 3.3 V.

Table continues on the next page...

Table 38. MC33902 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
6	EN	Input	Enable	MCU GPIO or SPI transmit data output	This is the enable input for the device in static mode control. This is the master output/slave input when used in SPI mode, and the MOSI (master out, slave in) during SPI operation.
7	INH	Output	Inhibit	Use depends on intended operation (see text below)	Inhibit output for control of an external power supply regulator
8	$\overline{\text{ERR}}$	Output	Active Low Error	MCU GPIO or SPI receive data input	Pin for static error and wakeup flag reporting MISO (master in, slave out) during SPI operation
9	WAKE	Input	Wake	MCU GPIO (output)	Wake input
10	VSUP	Input	Voltage Supply	Battery voltage	Battery supply pin, nominally 12 V
11	SPLIT	Output	Split	CAN termination midpoint	Output for connection of the CAN bus termination middle point
12	CANL	Input/output	CAN Bus Low	CAN Bus Connector	CAN bus low pin
13	CANH	Input/output	CAN Bus High	CAN Bus Connector	CAN bus high pin
14	$\overline{\text{NTSB}}$	Input	Standby	MCU GPIO or SPI Clock output	Standby input for device static mode control. CLK (Clock) during P_SPI operation

The use of the Inhibit pin (INH) is dependent on the selected target system operation. INH can turn an external power supply on and therefore wake a connected MCU for operation to save power when MCU operation is not required. In MPC5500 and MPC5600 automotive power train applications (engine control), INH is typically not used. However, in automotive body and chassis applications, it may be used.

8.4 FlexRay interface circuitry using TJA1080A

FlexRay is an automotive fault-tolerant 2-wire communications interface. FlexRay is generally used at 10,000 kbits/s (10 Mbit/s).

Freescale FlexRay devices implement a bus driver interface compliant with Communications System Electrical Physical Layer Specification, Version 2.1 Rev A.

Typically, FlexRay bus data rates of 10 Mbit/s, 8 Mbit/s, 5 Mbit/s, and 2.5 Mbit/s are supported and although the logic portions of the interface are implemented in the device, an external physical interface device is required to allow multiple FlexRay modules to be connected together.

The NXP™ (http://www.nxp.com) TJA1080A device is typically used as the FlexRay transceiver, although others are available. One transceiver is required for each FlexRay channel. The figure below shows the typical connections using the TJA1080A.

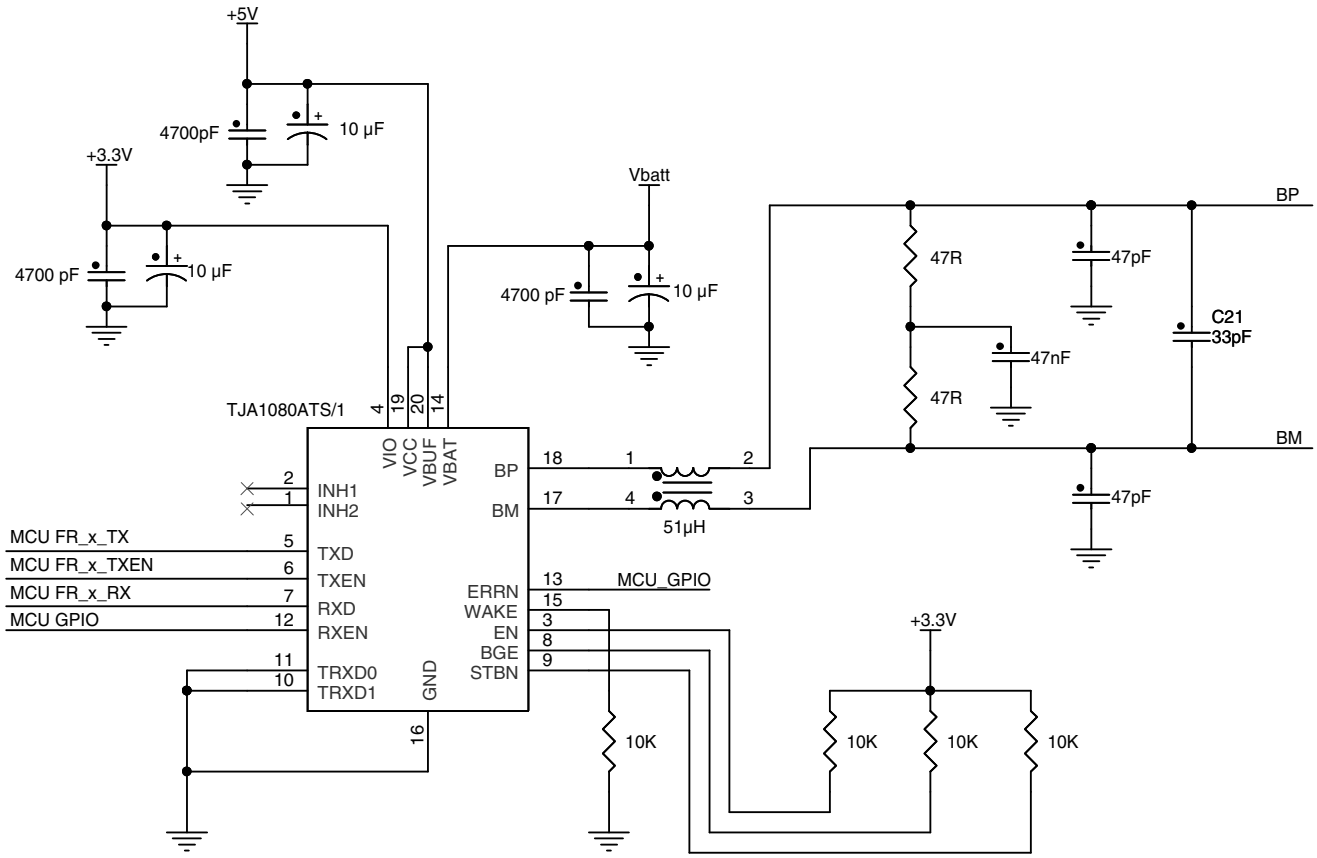


Figure 23. Typical FlexRay circuit

NOTE

Decoupling shown as an example only.

TRXD0/TRXD1 is pulled to ground to enable the transceiver as a node device (not star configuration)

In this configuration, only Normal mode is available. Further control is required to support Low-power mode.

MCU and system connections to the TJA1080A are shown in the following table.

Table 39. TJA1080 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	INH2	Output	Inhibit 2 Output	None	Inhibit output to enable/disable external power supply
2	INH1	Output	Inhibit 1 Output	None	Inhibit output to enable/disable external power supply
3	EN	Input	Enable Input	Pull up to 3.3 V or connect to a spare	Enable input (for mode selection

Table continues on the next page...

Table 39. TJA1080 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
				MCU GPIO (output to MCU)	(along with the STBN pin). Internal pulldown (transmitter disabled, but allows reception, listen only mode)
4	V_{IO}	Input (power)	IO Power Supply	3.3 V	Power supply input for the MCU I/O signals
5	TXD	Input	Transmit Data	MCU FR_x_TX	Transmit data from the MCU for transmitting on the FlexRay bus. Internal pullup
6	TXEN	Input	Transmit Enable	MCU FR_x_TXEN[1]	Transmit enable. A high level disables the transmitter. Internal pullup
7	RXD	Output	Receive Data	MCU FR_x_RX[1]	Receive data from the FlexRay bus to the MCU
8	BGE	Input	Bus Guardian Enable	Pull up to 3.3 V	The bus guardian input disables the transmitter. This feature is currently not supported
9	STBN	Input	Standby Input	Pull up to 3.3 V or connect to a spare MCU GPIO	Standby mode enable input (low to enter low power mode). Internal pulldown
10	TRXD1	Input/Output	Data Bus Line 1	Tie low	Data bus signal 1 for an inner star connection
11	TRXD0	Input/Output	Data Bus Line 0	Tie low	Data bus signal 0 for an inner star connection
12	RXEN	Output	Receive Enable	MCU GPIO (input to MCU)	Receive data enable indicates data is available from the bus (low during activity)
13	ERRN	Output	Error Output	MCU GPIO (input to MCU)	The error diagnostic output drives low upon an error
14	V_{BAT}	Input (power)	Battery Supply Voltage	Protected battery voltage	Battery supply voltage

Table continues on the next page...

Table 39. TJA1080 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
15	WAKE	Input	Local Wake Up Input	Tie low or connect to switch or MCU GPIO	The local wakeup input forces
16	GND	Input	Ground	Ground	Ground, power supply return reference
17	BM	Input/Output	Bus Line Minus	To FlexRay Connector	FlexRay bus minus signal
18	BP	Input/Output	Bus Line Plus	To FlexRay Connector	FlexRay bus plus signal
19	V_{CC}	Input (power)	Supply Voltage	5 V	Supply voltage for internal logic
20	V_{BUF}	Input (power)	Buffer Supply Voltage	5 V	Supply voltage for the FlexRay bus minus/plus signals

1. x can be A or B depending on the channel requirements in the system.

To support the requirements of different worldwide OEMs, two connector types for FlexRay are used on evaluation boards:

- One socket (female) DB-9 for both FlexRay channels
- Two Molex (Mini Fit Jr.™) headers, one for each FlexRay channel

However, there are various connectors used for production hardware. The tables and figures below show example pinouts for both connector types. The DB-9 connector allows for two channels on a single connector. The dual channels allow for redundant wiring for increased reliability. The dual channel capability is built into the FlexRay standard.

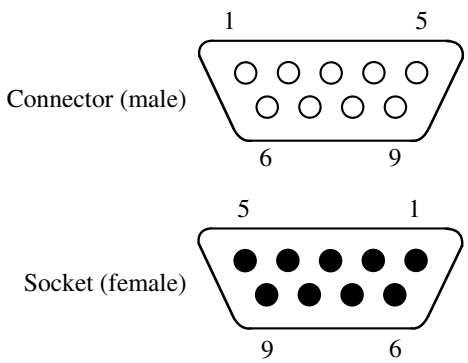


Figure 24. DB-9 connector and socket

Table 40. DB-9 pin-signal mapping

Pin Number	Signal Name	Full Name/Description
1	N/C	No connection
2	BM_A	Bus Minus Channel A
3	GND	No connection
4	BM_B	Bus Minus Channel B
5	SHIELD (OPTIONAL)	Optional Shield (if required)

Table continues on the next page...

Table 40. DB-9 pin-signal mapping (continued)

Pin Number	Signal Name	Full Name/Description
6	N/C	No connection
7	BP_A	Bus Plus Channel A
8	BP_B	Bus Plus Channel B
9	N/C	No connection

NOTE

A socket (female) is used on the evaluation board and a cable with a connector (male) connects with this.

The metal shell of the socket should be connected through a ferrite bead to GND.

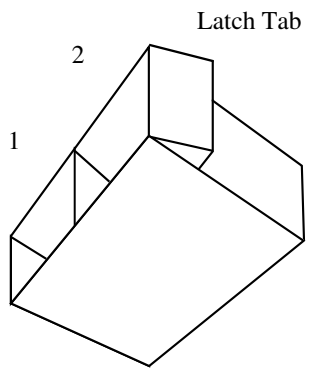


Figure 25. Molex connector picture

Table 41. Molex pin-signal mapping

Pin Number	Signal Name
1	BP
2	BM

NOTE

A connector (male) is used on the evaluation board and a cable with a socket (female) connects with this.

The Molex connectors are available in two types, one with pegs for mounting to the board and one without. The part numbers are shown in the following table.

Table 42. Recommended Molex Mini-Fit Jr. connector part numbers

Description	Manufacturer Part Number (Molex)
2-pin vertical connector with pegs for target system, tin contacts, latch	39-29-9022
2-pin vertical connector without pegs for target system, tin contacts, latch	39-28-8020

Table continues on the next page...

Table 42. Recommended Molex Mini-Fit Jr. connector part numbers (continued)

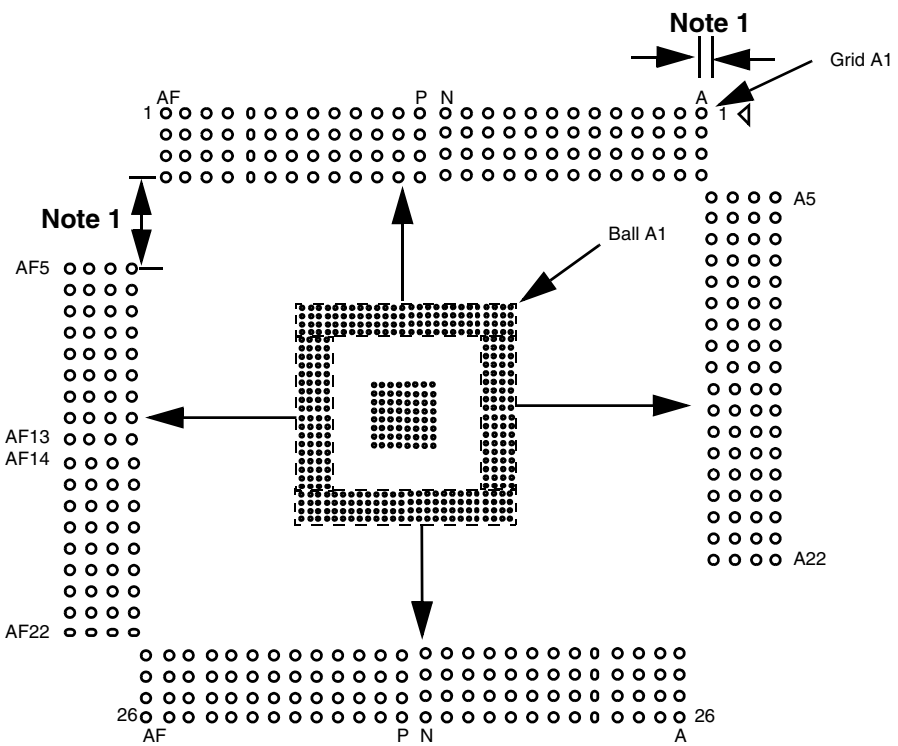
Description	Manufacturer Part Number (Molex)
2-pin right-angle connector with pegs for target system, tin contacts, latch	39-30-0020
2-pin right-angle connector with flange for target system, tin contacts, latch	39-29-1028
Mating connector with latch for cable assemblies	39-01-2020
Female terminal for mating cable assembly	39-00-0077

9 EVB Pin access

Access to all of the pins of the MPC5500 devices are available on an I/O header ring on the device Evaluation Board (EVB). The pin-out of this I/O ring is the same as the pin-out of the device, except that parts of the ring have been moved outward to make room for the part and socket on the EVB. The figure below shows the configuration of the pin access.

NOTE

It is not a good design practice to include access to all pins in this manner since each of these pins becomes an antennae. This and the additional trace lengths will generate excessive electromagnetic energy (EMC).



Notes:
1. Maintain 0.1 inch grid on all pin headers

Figure 26. MPC5500 EVB I/O pin access

The following pins are not connected to the I/O header ring: EXTAL, XTAL, VRCCTL, VDDSYN, VSSSYN, and REFBYPC. Connections to these pins are considered critical to the proper operation of the device. All VSS, VDD, and 3.3 V pins are connected directly to the board's respective board plane.

10 References

More information can be found in the documents shown in the table below.

Table 43. References

Document Number	Document title	Location
MPC5534RM	MPC5534 Reference Manual	www.freescale.com
MPC5553_MPC5554_RM	MPC5553/5554 Reference Manual	
MPC5561RM	MPC5561 Reference Manual	
MPC5565RM	MPC5565 Reference Manual	
MPC5566RM	MPC5566 Reference Manual	
MPC5567RM	MPC5567 Reference Manual	
MPC5534	MPC5534 Data Sheet	
MPC5553	MPC5553 Data Sheet	
MPC5554	MPC5554 Data Sheet	
MPC5561	MPC5561 Data Sheet	
MPC5565	MPC5565 Data Sheet	
MPC5566	MPC5566 Data Sheet	
MPC5567	MPC5567 Data Sheet	
AN2614	Nexus Interface Connector Options for the MPC5500 Family	
AN2705	Signal Integrity Considerations with MPC5500-based Systems	
AN2706	EMC Guidelines for MPC5500-based Systems	

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number AN2613
Revision 0, August 21, 2013